SONY

CXD2552Q

1 Bit D/A Converter

Description

The CXD2552Q is 1 bit type D/A converter developed for digital audio products; compact disc player and others.

44 pin QFP (Plastic)

Features

- PLM pulse converter
- 3rd order noise shaper
- Direct digital sync
- Master clock 1024Fs
- 2 channel built in

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +6.5 V
- Input voltage V_I −0.3 to V_{DD}+0.3 V
- Allowable power dissipation
  P_D 500 mW (Ta=60°C)
- Storage temperature
  Tstg −55 to +150 °C

Structure

Silicon gate CMOS IC

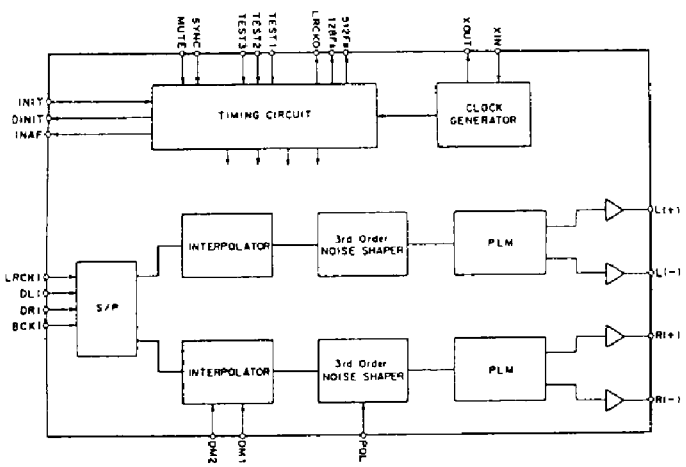
Applications

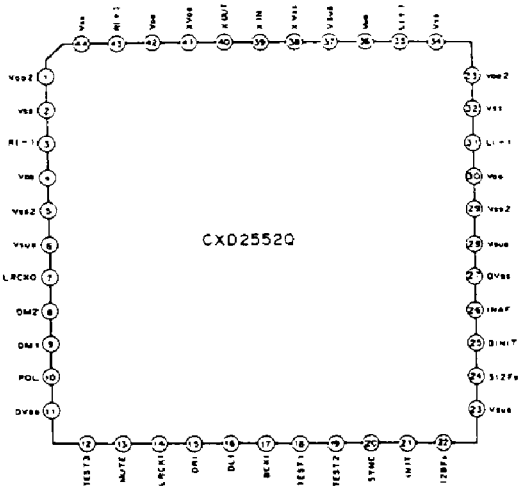
Compact disc player, digital amplifier, BS tuner

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25 V
- Operating temperature Topr −10 to 60 °C
- OSC frequency fx 32.0 to 49.7 MHz
- Supply voltage difference
  V_{DD}–V_{DD2}, V_{DD}–DV_{DD}, V_{DD}–XV_{DD} ± 0.1V
  V_{SS}–V_{SS2}, V_{SS}–DV_{SS}, V_{SS}–XV_{SS} ± 0.1V

Block Diagram and Pin Configuration





Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD2}	—	Analog power supply
2	Vss	—	Analog GND
3	R (–)	O	Rch PLM output (Opposite phase)
4	V_{DD}	—	Analog power supply
5	V_{SS2}	—	Analog GND
6	V_{SUB}	—	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV_{DD}	—	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin.Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V_{SUB}	—	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DVss	—	Digital GND
28	V_{SUB}	—	Sub straight. Connect to GND.
29	V_{SS2}	—	Analog GND
30	V_{DD}	—	Analog power supply
31	L (–)	O	Lch PLM output (Opposite phase)
32	Vss	—	Analog GND
33	V_{DD2}	—	Analog power supply
34	Vss	—	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V_{DD}	—	Analog power supply
37	V_{SUB}	—	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	——	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XV_{DD}	——	Clock power supply
42	V_{DD}	——	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	Vss	——	Analog GND

Electrical Characteristics

DC Characteristics

($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60°C)

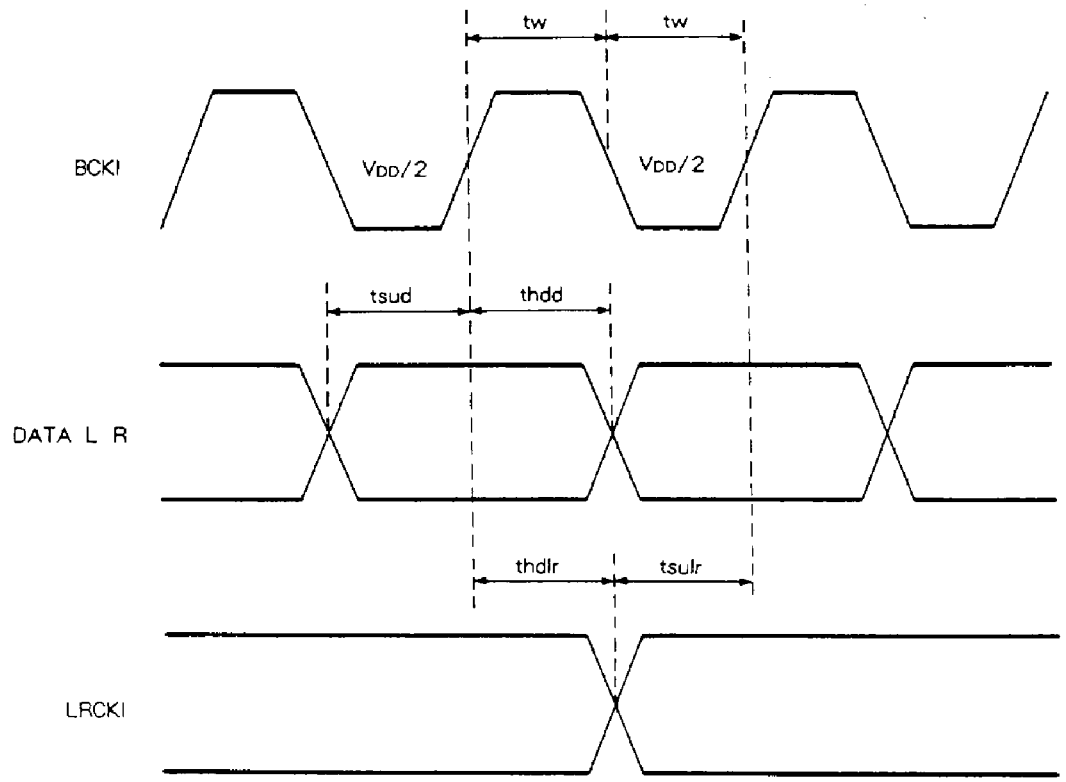
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	——	0.76V_{DD}			V
"L" input voltage	V_{IL}	——			0.24V_{DD}	V
Input leak current	I_{LI}	——			± 5.0	µA
"H" output voltage (DINIT, INAF)	V_{OH}	Io=−1mA	V_{DD}−0.5			V
"L" output voltage (DINIT, INAF)	V_{OL}	Io=1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V_{OH}	Io=−0.4mA	V_{DD}−0.5			V
"L" output voltage(512Fs, LRCKO)	V_{OL}	Io=0.4mA			0.4	V
"H" output voltage (128Fs)	V_{OH}	Io=−0.3mA	V_{DD}−0.5			V
"L" output voltage (128Fs)	V_{OL}	Io=0.3mA			0.4	V
"H" output voltage (R+, R−, L+, L−)	V_{OH}	Io=−15mA	V_{DD}−0.5			V
"L" output voltage (R+, R−, L+, L−)	V_{OL}	Io=15mA			0.5	V
"H" output voltage (XOUT)	V_{OH}	Io=−2.0mA	V_{DD}−0.5			V
"L" output voltage (XOUT)	V_{OL}	Io=2.0mA			0.4	V
Current consumption	I_{DD}	——		55	80	mA

AC Characteristics

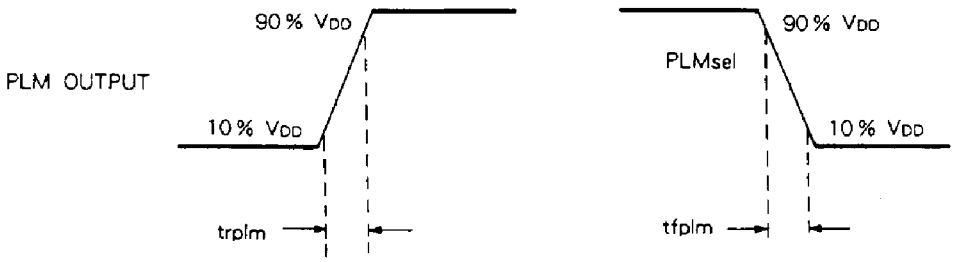
($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw		38			nsec
DATAL, R set up time	tsud		18			nsec
DATAL, R hold time	thdd		18			nsec
LRCKI set up time	tsulr		18			nsec
LRCKI hold time	thdlr		18			nsec
PLM output rise/fall time	tr, tf	CL=300pF		10		nsec

• Input



• Output



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Analog Characteristics ($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	1kHz, 0dB/– ∞ dB data (Fs=44.1kHz) (A filte used)	96			dB

Electrical Characteristics Testing Method

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

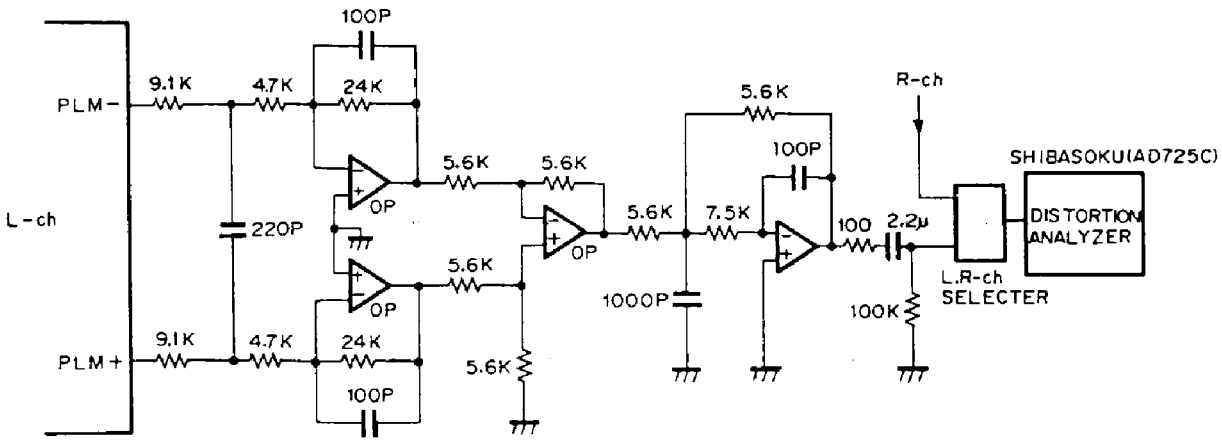


Fig. 1.

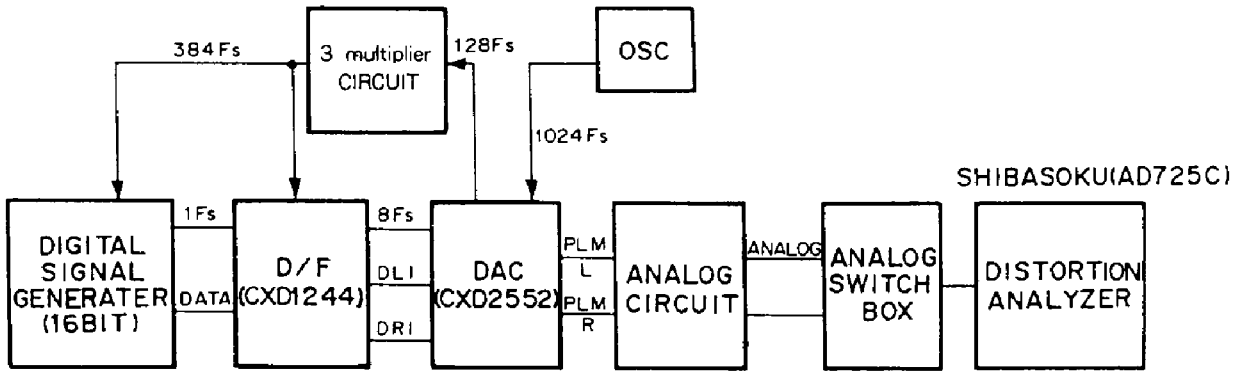


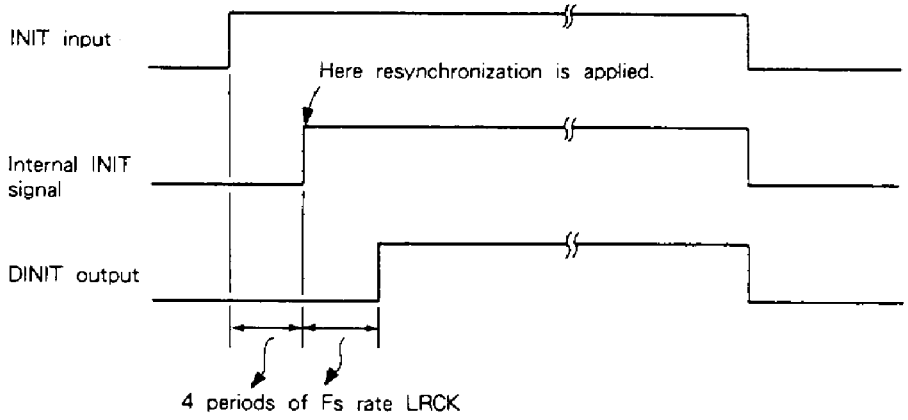
Fig. 2.

Description of Function

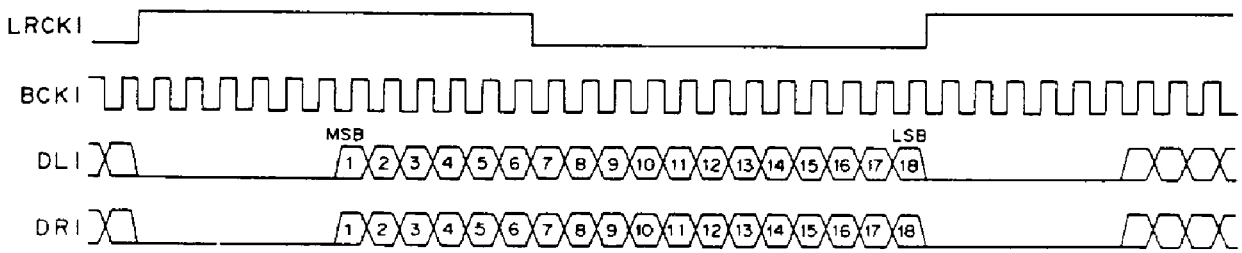
I/O Synchronizing Circuit

1) Theory of operation
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK ↓) of the LRCK input has entered the window or not.
When power supply is turned on, should LRCK ↓ be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK ↓. Synchronization between the exterior system and this LSI is established through this operation.

2) Resynchronization by means of INIT
Even when LRCK ↓ is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK ↓ is located at the center of the window.
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.



Input Timing (8fs rate)



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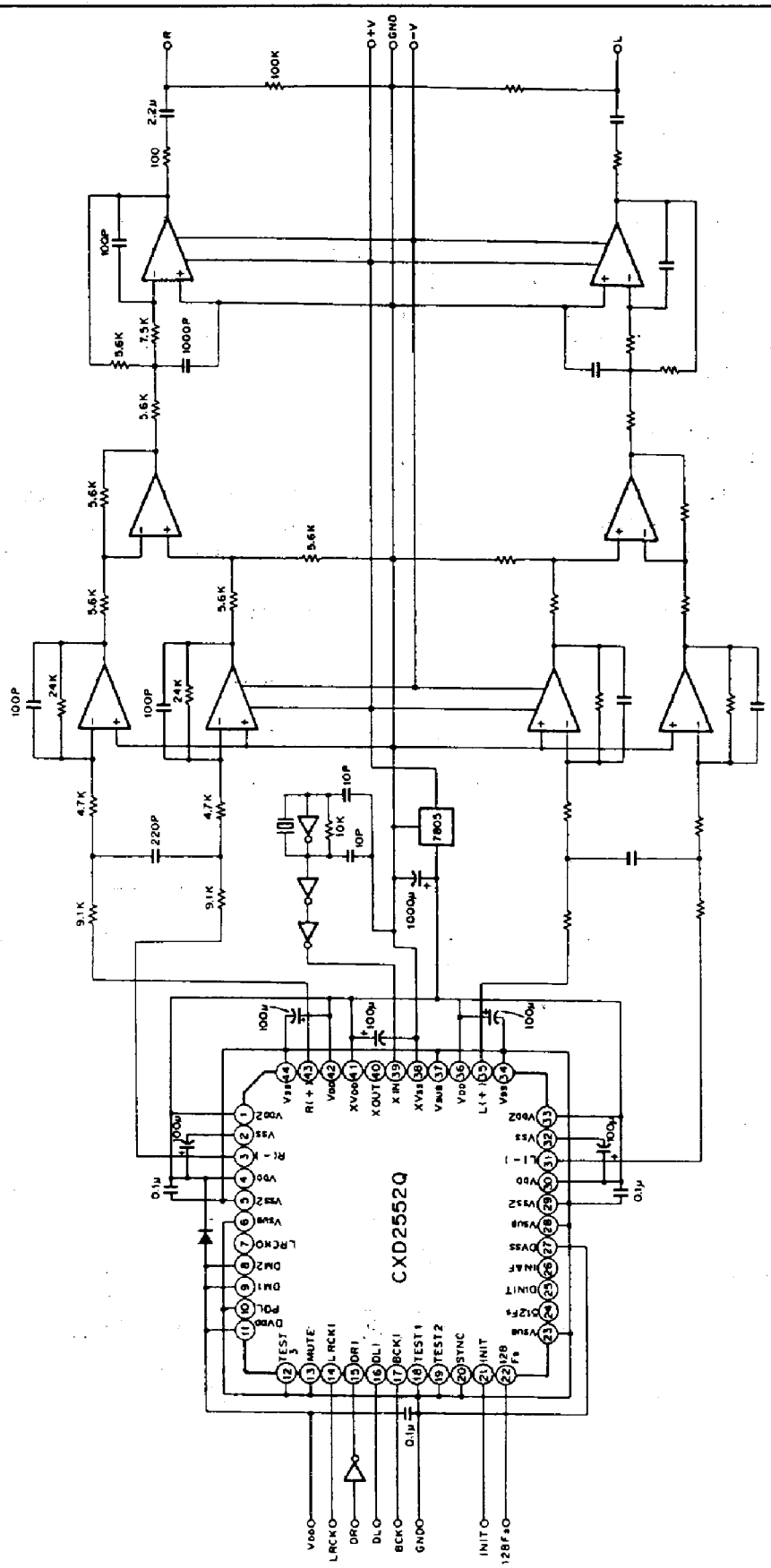
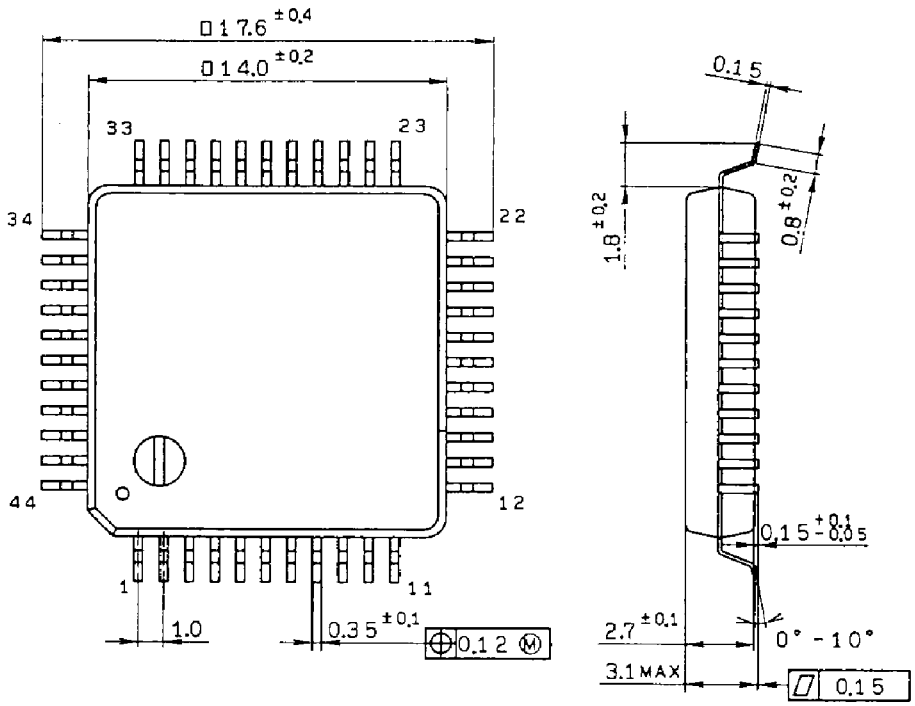
Application Circuit



Package Outline Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	———

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