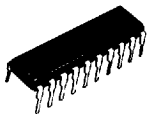
LC78820, 78820M


3021B


3036B

CMOS LSI

Two-channel 18-bit D/A Converter for Digital Audio

OVERVIEW

The LC78820 and LC78820M are two-channel 18-bit D/A converters designed for digital audio applications. They use two, independent dynamic level-shift converters, each comprising a 512-element resistor string, a 3-bit PWM circuit and a 6-bit level shifter.

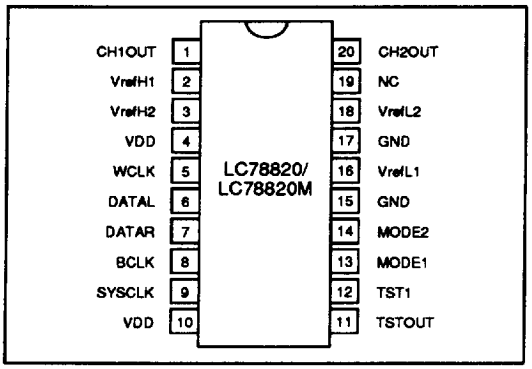
The LC78820 and LC78820M read 2s complement input serial data at a sampling rate (eight-times oversampling) of 384 kHz. They generate minimal total harmonic distortion of 0.08% maximum (0.05% for selected devices) with good channel separation and excellent signal-to-noise ratio. The channel outputs are synchronized and feature zero phase difference.

The LC78820 and LC78820M operate from a single 5 V supply and are available in 20-pin DIPs or MFPs.

FEATURES

- 2s complement serial input data
- Two-channel 18-bit D/A conversion
- Zero phase difference between left and right channels
- Eight-times oversampling of 384 kHz
- No external sample-and-hold circuit
- Low-power silicon-gate CMOS process
- Single 5 V supply
- 20-pin DIP or 20-pin MFP

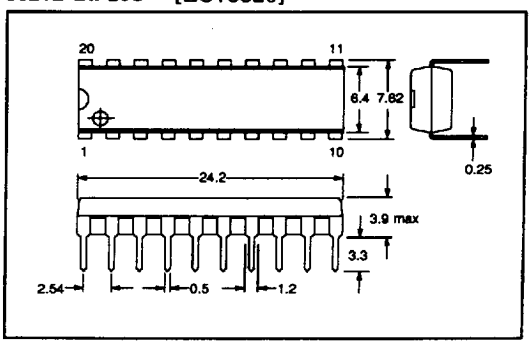
PINOUT



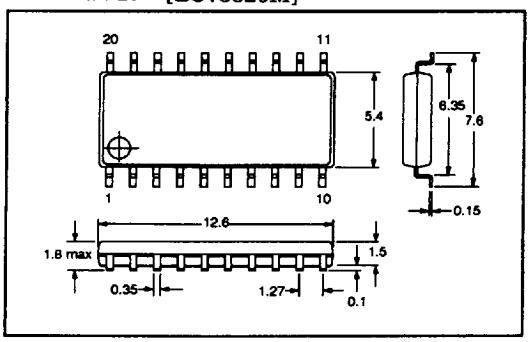
PACKAGE DIMENSIONS

Unit: mm

3021B-DIP20S [LC78820]

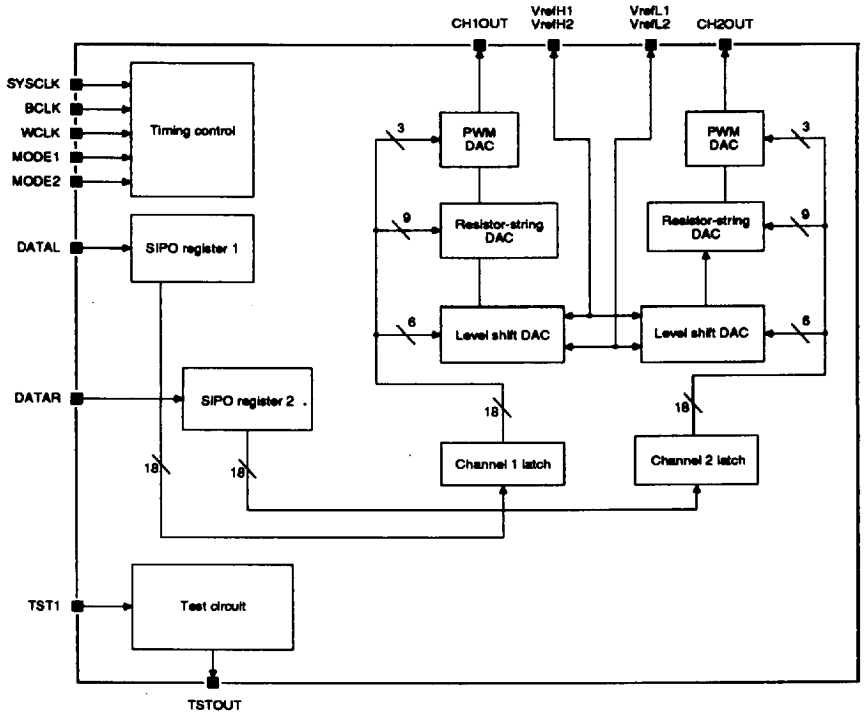


3036B-MFP20 [LC78820M]



BLOCK DIAGRAM

SANYO SEMICONDUCTOR CORP



PIN DESCRIPTION

Number	Name	Description
1	CH1OUT	Left-channel pulsewidth modulated output signal
2	VrefH1	HIGH-level input reference voltage 1
3	VrefH2	HIGH-level input reference voltage 2
4	VDD	Supply voltage
5	WCLK	Latch data word clock
6	DATAL	Left-channel serial data input (most significant bit first)
7	DATAR	Right-channel serial data input (most significant bit first)
8	BCLK	Serial data bit clock
9	SYSCLK	System clock. Selects the word clock polarity in some timing modes
10	VDD	Supply voltage
11	TSTOUT	Output test pin (normally open)
12	TST1	Input test pin (normally grounded)
13	MODE1	Serial input data and timing mode selection 1
14	MODE2	Serial input data and timing mode selection 2
15	GND	Ground

Number	Name	Description
16	VrefL1	LOW-level input reference voltage 1
17	GND	Ground
18	VrefL2	LOW-level input reference voltage 2
19	NC	Not connected
20	CH2OUT	Right-channel pulsewidth modulated output signal

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{opg}	–30 to 75	°C
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5.0	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

Electrical Characteristics

V_{DD} = 5.0 V, T_a = 25 deg. C unless otherwise noted

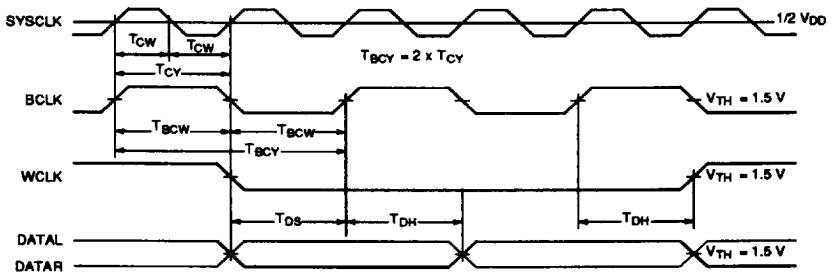
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level reference voltage	V_{refL}		0	–	0.5	V
HIGH-level reference voltage	V_{refH}		V_{DD} – 0.5	–	V_{DD}	V
SYSCLK LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
LOW-level input voltage, all other pins	V_{IL2}		–0.3	–	0.8	V
SYSCLK HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
HIGH-level input voltage, all other pins	V_{IH2}		2.2	–	V_{DD} + 0.3	V
Power consumption	P_d		–	–	60	mW
Resolution	RES		–	18	–	bits
Sampling frequency	F_s		–	–	384	kHz
Total harmonic distortion	THD	1 kHz, 0 dB gain	–	–	0.08	%
		1 kHz, 0 dB gain. See note 2.	–	–	0.05	

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Crosstalk	CT	1 kHz, 0 dB gain	–	–85	–	dB
Signal-to-noise ratio	S/N		–	92	–	dB

Notes

1. Measurements are taken with a sampling frequency of F_S = 384 kHz using the typical application circuit shown in figure 6.
2. Selected devices

Timing Characteristics



Parameter	Symbol	Rating			Unit
		min	typ	max	
System clock pulsewidth	T_{CW}	25	–	–	ns
Bit clock pulsewidth	T_{BCW}	35	–	–	ns
Data setup time	T_{DS}	25	–	–	ns
Data hold time	T_{DH}	25	–	–	ns

FUNCTIONAL DESCRIPTION

The LC78820 and LC78820M have two, independent D/A converter channels, each comprising a serial-to-parallel converter, a latch and an 18-bit level-shift D/A converter. Each 18-bit data word is split into three fields—D0 to D5, D6 to D8 and D9 to D17—with each field controlling one part of the D/A converter as shown in figure 1.

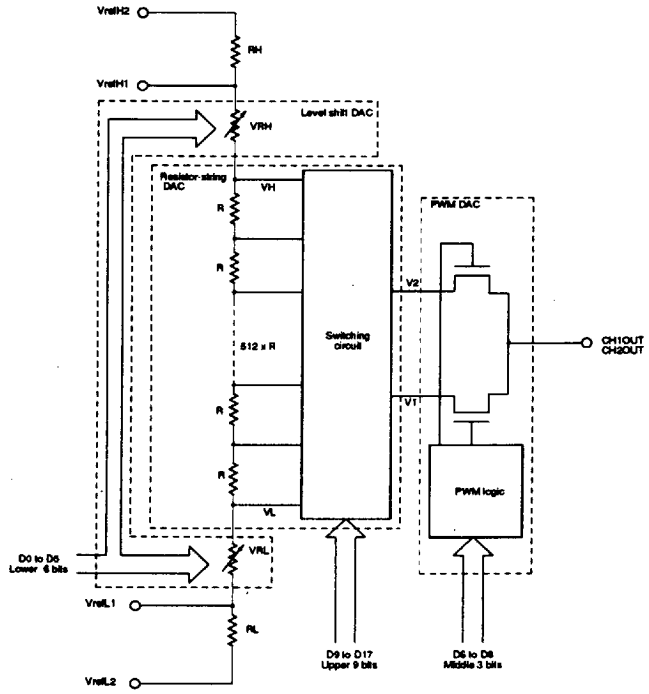


Figure 1. D/A converter

Resistor String and Switching Circuit

The resistor-string voltage divider comprises 512 equal-value resistors and is driven by the upper nine bits (D9 to D17) of the input word. The switching circuit selects a pair of adjacent taps from the string and passes them to the PWM circuit, shown as V1 and V2 above. The difference between these voltages is (VH – VL) / 512, where VH and VL are the HIGH- and LOW-level reference voltages, respectively.

PWM Circuit

The PWM circuit switches the output voltages at V1 and V2. The duty cycle is controlled by the middle three bits (D6 to D8) of the input word. The average output voltage is equal to one of the eight equally-spaced voltage levels between V1 and V2.

Level Shifter

The level shifter adjusts the voltages along the resistor string by changing the resistances VRH and VRL. These are controlled by the least-significant six bits (D0 to D5) of the input word.

VRH and VRL are changed in steps of R / 512, where R is the value of each resistor in the string. The sum of VRH and VRL is a constant.

The level shifter shifts both V1 and V2 between 0 and (63 × ΔV) / 512 volts in ΔV / 512 volt steps, where ΔV = VH – VL.

TIMING MODES

The LC78820 and LC78820M operate in one of four timing modes, as selected by the voltages on MODE1 and MODE2. The bit clock, BLCK, and system clock, SYSCLK, are shown in figures 2, 3, 4 and 5 for each mode as a multiple of the sampling frequency, F_s.

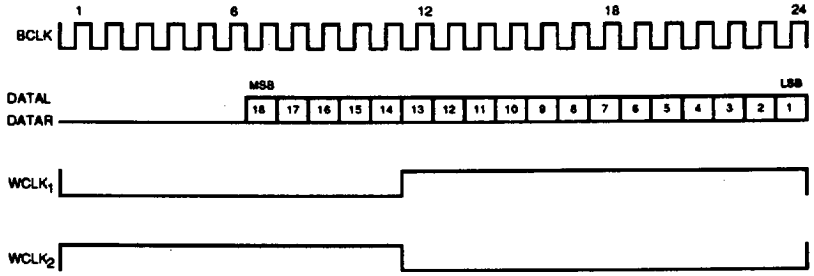


Figure 2. Timing mode 1: MODE1 = LOW, MODE2 = LOW

Notes

1. When SYSCLK is LOW, the word clock is $WCLK_1$, and when HIGH, $WCLK_2$.
2. BCLK = 24 × F_s, where F_s = 8 × f_s

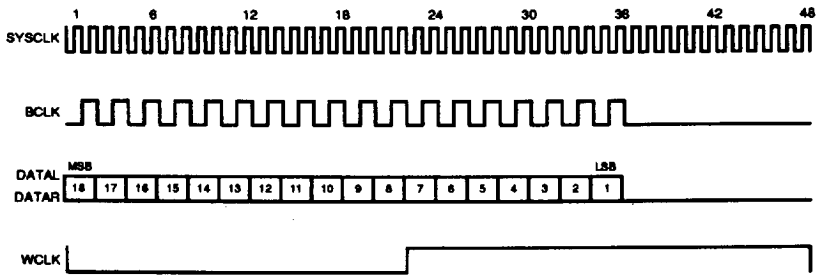


Figure 3. Timing mode 2: MODE1 = LOW, MODE2 = HIGH

Note

SYSCLK = 48 × F_s, where F_s = 8 × f_s

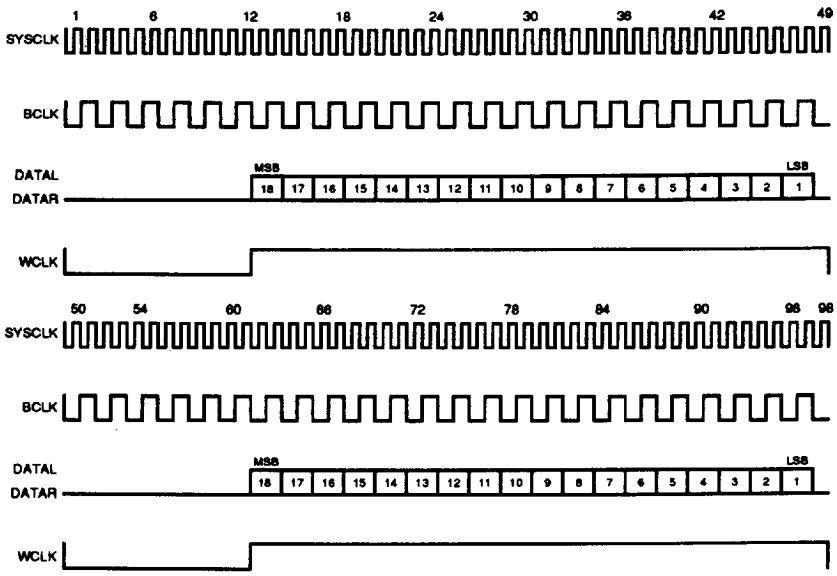


Figure 4. Timing mode 3: MODE1 = HIGH, MODE2 = LOW

Note
SYSCLK = 49 × F_s, where F_s = 8 × f_s

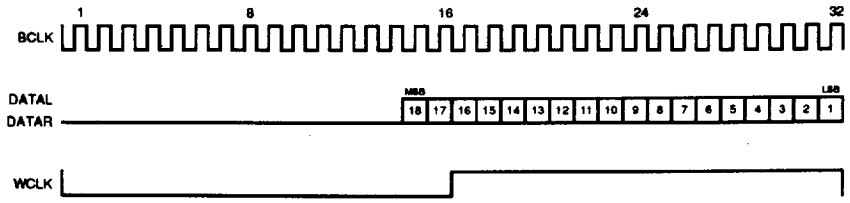


Figure 5. Timing mode 4: MODE1 = HIGH, MODE2 = HIGH

Note
BCLK = 32 × F_s, where F_s = 8 × f_s

DESIGN INFORMATION

Ground Lines

Ensure that the digital and analog ground lines are separate, and that DGND and AGND are connected correctly.

Supply Voltage

Use a low regulation, low-impedance supply. Connect both VDD pins to the same supply to prevent possible latch-up caused by different V_{DD} supply voltages.

Reference Voltage

Use a low-noise voltage source for V_{ref}. The most common reference voltage connection is V_{refH1} = 5 V and V_{refL1} = 0 V, with VrefL2 and VrefH2 open circuited.

Output Buffers

Use output buffer op-amps since both CH1OUT and CH2OUT have high output impedances. When the reference voltage connection is V_{refH2} = 5 V and V_{refL2} = 0 V, an op-amp buffer should be connected to the output, and 47 µF capacitors, between both VrefL1 and VrefH1, and GND.

The maximum peak output voltage, when the R_H and R_L internal resistors are in use, ranges from 1.5 to 3.5 V.

TYPICAL APPLICATIONS

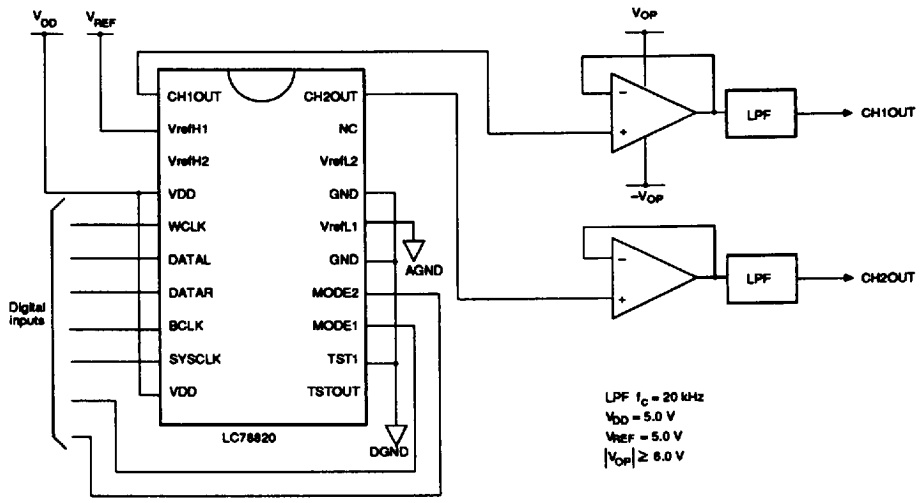


Figure 6. DC-coupled D/A converter

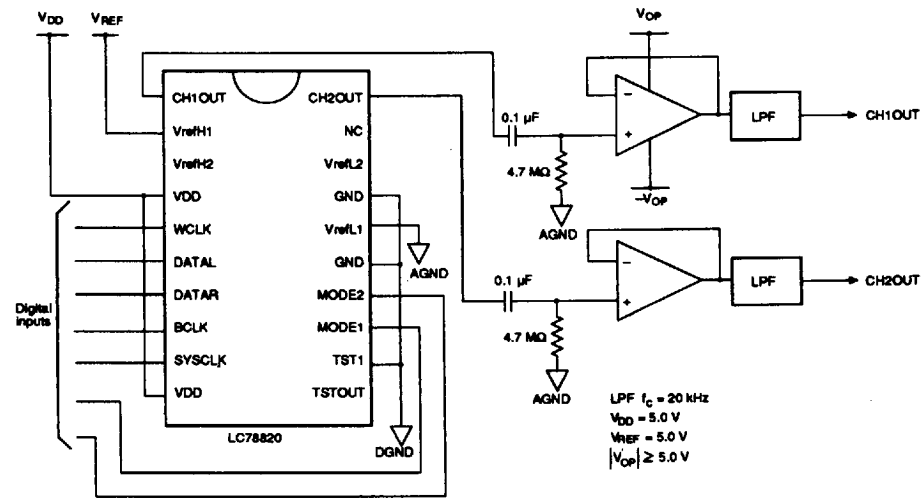


Figure 7. AC-coupled D/A converter

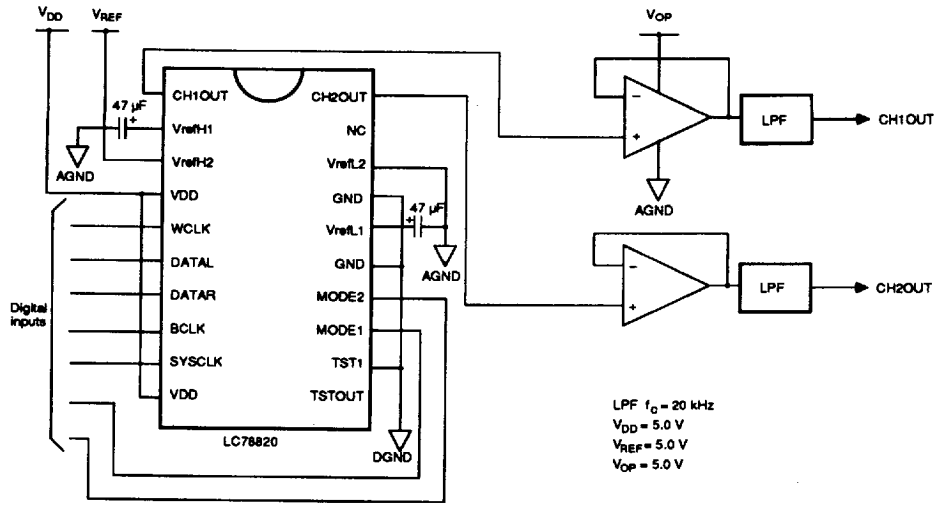


Figure 8. DC-coupled single-ended supply D/A converter