COMPACT DISC CIRCUIT SAA7000

GENERAL DESCRIPTION

The SAA7000 interpolation and muting circuit descrambles and separates data into left and right channels and minimizes the effects of erroneous data on the performance of the Compact Disc Digital Audio System. Minor errors (those present in one data sample only) are replaced with audio data obtained by interpolation; more persistent errors are removed by muting.

Features

- Descrambles data from error corrector SAA7020 and formats into left and right channels
- Minimizes the effect of erroneous data samples
- 16-bit serial data input (two's complement)
- Smoothed transitions before and after muting
- Interpolated data replaces single erroneous data samples
- Serial output for digital-to-analogue converters (DACs) or filter circuits
- Generates crystal-derived timing signals for system master data clock (4,2336 MHz), serving error corrector SAA7020 and digital filter SAA7030
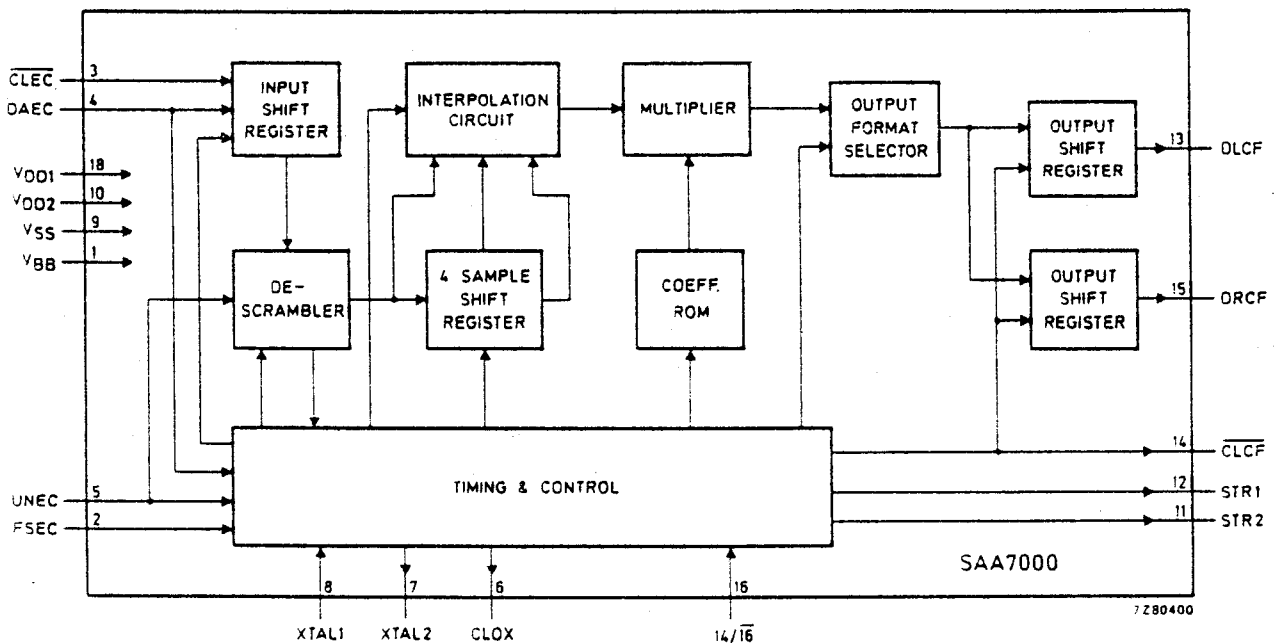- Selectable output format: offset binary or two's complement; 14 or 16-bit word

3

Fig. 1 Block diagram.

PACKAGE OUTLINE
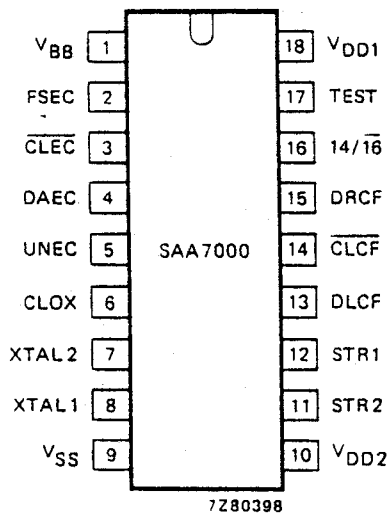
18-lead DIL; plastic (SOT-102CS).

COMPACT DISC CIRCUIT

Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	FSEC	frame sync pulse input
3	$\overline{CLEC}$	input data clock
4	DAEC	data input (two's complement) and output format selector
5	UNEC	error flag input
6	CLOX	buffered clock output (XTAL1)
7	XTAL2	drive output to clock crystal
8	XTAL1	external clock input
9	V_{SS}	ground
10	V_{DD2}	+ 12 V supply
11	STR2	strobe 2 output
12	STR1	strobe 1 output
13	DLCF	left channel data output (format selected by DAEC)
14	$\overline{CLCF}$	14/16-bit clock burst output
15	DRCF	right channel data output (format selected by DAEC)
16	$14/\overline{16}$	selects bit length of clock burst output from $\overline{CLCF}$
17	TEST	test input
18	V_{DD1}	+ 5 V supply

FUNCTIONAL DESCRIPTION

The SAA7000 is used in the Compact Disc system to reconstruct audio data by interpolation if the error corrector SAA7020 is unable to correct a data sample, or mutes the data when it passes consecutive erroneous data samples. Errors are indicated by an error flag (UNEC) from the SAA7020; when no error flag occurs, the data value through SAA7000 is unaffected.

Data samples (at DAEC, clocked in by $\overline{CLEC}$) are first descrambled and then separated into left and right channels. A similar descramble and separation is performed on the error flag (UNEC).

If, for either left or right channels, a single 'error' is flagged between two 'good' data samples then linear interpolation is used to replace the erroneous value. If two or more adjacent samples are flagged, then the samples in error are muted. Beginning thirty samples before the first of the consecutive errors, the data value of the samples is attenuated smoothly to zero following a (0 to π) cosine curve. After the error burst, the next thirty samples are smoothly returned to full level following a (π to 2π) cosine curve. The muting is applied simultaneously to data in both left and right channels regardless of the source of the error.

The data (good or processed) is formatted into two's complement or offset binary to match the DACs in use. This selection is made with a special function of the data input (DAEC, see Fig. 6). The data is then fed to the left and right outputs (DLCF and DRCF) and is clocked out by the output clock ($\overline{CLCF}$). Strobes (STR1 and STR2) are generated for the DACs and the digital filter (SAA7030). Fourteen or sixteen-bit DACs can be accommodated by the use of the select input ($14/\overline{16}$).

The SAA7000 automatically synchronizes to the error detector SAA7020 output using the frame sync pulse (FSEC) for internal timing reset and feeds a 2 x bit-rate clock (CLOX) to the system.

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COMPACT DISC CIRCUIT

SAA7000

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	FSEC	Frame sync pulse (active HIGH) received from SAA7020 at the start of a data frame (12 data samples). FSEC is used to synchronize the descrambler to the data frames. For re-synchronization to occur, two consecutive FSEC pulses must be received each having a pulse width of approximately 6 CLOX cycles and the leading edge of the second pulse must be one data frame later than that of the first. FSEC is also used to synchronize the internal clock to the $\overline{CLEC}$ clock input, so aligning the gap in the internal clock to the FSEC pulse (see Fig. 4).
3	$\overline{CLEC}$	Input data clock used to load serial data at DAEC into the input shift register. After a data sample has been loaded $\overline{CLEC}$ is held LOW to give a gap of 16 CLOX cycles (see Fig. 4). The period of the $\overline{CLEC}$ clock is 2 x the period of a CLOX cycle.
4	DAEC	Serial data samples are received at DAEC in two's complement form. The data is in 16-bit words separated by gaps; each word comprising two 8-bit symbols. The DAEC input is also used to select the output format; during the $\overline{CLEC}$ gap, a HIGH level at DAEC selects two's complement and a LOW level selects offset binary format (see Fig. 4).
5	UNEC	Error flag indicating unreliable data from SAA7020. During the period when data is clocked in at DAEC, UNEC is LOW only if the present 8-bit symbol is valid. During the period of the $\overline{CLEC}$ gap, UNEC is LOW only if the whole of the data word due to arrive 5 frames later is valid.
6	CLOX	Buffered XTAL1 clock output.
7	XTAL2	Main clock crystal drive output. This pin should remain disconnected if a crystal is not used.
8	XTAL1	Clock input from crystal circuit or for externally derived clock.
9	V_{SS}	Ground (0 V).
10	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
11	STR2	Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 24 CLOX cycles and used to strobe data to the DACs. This pin should be left disconnected if SAA7030 is not used.
12	STR1	Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 96 CLOX cycles — after each pair of data words have been clocked out. It is used to strobe data to SAA7030, or to the DACs if SAA7030 is not used. Both STR1 and STR2 are re-synchronized to XTAL1 to minimize jitter.
13	DLCF	Left channel data output; format in two's complement or offset binary, as selected at DAEC.
14	$\overline{CLCF}$	Clock burst output of either 14 or 16 bits, as selected at pin 16. It is used to clock data from DLCF and DRCF (data is valid on $\overline{CLCF}$ falling edge, see Fig. 5).
15	DRCF	Right channel data output; format is two's complement or offset binary, as selected at DAEC.
16	$14/\overline{16}$	Selects 14 or 16-bit bursts of output clock $\overline{CLCF}$.

3

| 17 | TEST | This pin should be held LOW to ensure normal operation. |
| 18 | V_{DD1} | Positive supply voltage: $+5$ V $\pm$ 10%. |

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); $V_{SS} = 0$ V

Supply voltage 1 range (pin 18)	V_{DD1}	$-0,3$ to $+7,5$	V
Supply voltage 2 range (pin 10)	V_{DD2}	$-0,3$ to $+15$	V
Back bias supply voltage range (pin 1)	V_{BB}	-4 to $+0,3$	V
Input voltage range	V_I	$-0,3$ to $+7,5$	V
Output voltage range at $V_I = -0,3$ to $+6,5$ V; $T_{amb} = 25\ ^oC$	V_O	$-0,3$ to $+7,5$	V
Output current	I_O	max. $\quad$ 10	mA
Operating ambient temperature range	T_{amb}	-20 to $+70$	^oC
Storage temperature range	T_{stg}	-55 to $+125$	^oC

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COMPACT DISC CIRCUIT

CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = -20$ to $+70$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 18)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 10)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 18)	I_{DD1}	30	70	140	mA
Supply current 2 (pin 10)	I_{DD2}	2	5	10	mA
Back bias supply current (pin 1)	$-I_{BB}$	–	–	500	μA
Inputs (except V_{BB})					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,4	–	6,5	V
Input current (note 1)	I_I	−1	–	+ 1	μA
Input capacitance (not XTAL1)	C_I	–	–	7	pF
Outputs DLCF, DRCF, $\overline{\text{CLCF}}$, CLOX, STR1, STR2 (note 2)					
Output voltage LOW at $-I_{OL} = 1,6$ mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $I_{OH} = 0,2$ mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	–	150	pF
Output XTAL2					
Operating frequency using crystal oscillator (Fig. 3)	f_{XTAL}	3,0	4,2336	4,5	MHz
Operating frequency using driven input applied to XTAL1	f_{IN}	3,0	4,2336	4,5	MHz
Input XTAL1					
Input clock LOW	t_{IXL}	40	–	–	% of period
Input clock HIGH	t_{IXH}	40	–	–	
Crystal amplifier (pins 7 and 8)					
Mutual conductance at 5 MHz	gm	1,5	–	–	mA/V
Bandwidth of mutual conductance at minimum 3 dB	B_{gm}	10	–	–	MHz
Input capacitance	C_I	–	–	10	pF
Output capacitance	C_O	–	–	7	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Input leakage current	I_I	−1	–	+ 1	μA
Output current at 5 MHz	I_o	−1	–	+ 1	mA
Small signal gain at 5 MHz	A_V	−4	–	–	

COMPACT DISC CIRCUIT

parameter	symbol	min.	typ.	max.	unit
Inputs DAEC, UNEC, $\overline{CLEC}$, FSEC					
Input rise time (FSEC only)	t_{IR}	—	—	100	ns
Input fall time (FSEC only)	t_{IF}	—	—	100	ns
$\overline{CLEC}$ HIGH	t_{ICH}	100	—	—	ns
$\overline{CLEC}$ LOW	t_{ICL}	100	—	—	ns
DAEC to $\overline{CLEC}$ set-up time	t_{IDS}	40	—	—	ns
$\overline{CLEC}$ to DAEC hold time	t_{IDH}	40	—	—	ns
FSEC HIGH (note 3)	t_{FSH}	4 CLOX periods −400	—	8 CLOX periods +190	ns
DAEC/UNEC to FSEC set-up time	t_{UFS}	0	—	—	ns
FSEC to DAEC/UNEC hold time (note 3)	t_{UFH}	8 CLOX periods +325	—	—	ns
Output CLOX (notes 4 and 5)					
Output clock LOW	t_{OXL}	30	—	—	% of period
Output clock HIGH	t_{OXH}	30	—	—	% of period
output clock rise time	t_{OXR}	—	—	50	ns
Output clock fall time	t_{OXF}	—	—	40	ns
Outputs STR1, STR2 (note 6)					
Output strobe rise time	t_{OSR}	—	10	20	ns
Output strobe fall time	t_{OSF}	—	6	20	ns
Output strobe HIGH	t_{OSH}	1 CLOX period +50	2 CLOX periods −20	4 CLOX periods	ns
Output strobe LOW	t_{OSL}	10	—	—	CLOX periods
CLOX to STR1, STR2 delay time	t_{XSL}	0	—	—	ns
	t_{XSH}	—	—	45	ns

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COMPACT DISC CIRCUIT

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs $\overline{CLCF}$, DLCF, DRCF (note 4)					
Output rise time	t_{OR}	–	–	50	ns
Output fall time	t_{OF}	–	–	40	ns
Output data clock HIGH	t_{OCH}	120	–	–	ns
Output data clock LOW	t_{OCL}	120	–	–	ns
DLCF, DRCF to $\overline{CLCF}$ set-up time	t_{ODS}	50	–	–	ns
$\overline{CLCF}$ to DLCF, DRCF hold time	t_{ODH}	100	–	–	ns
$\overline{CLCF}$ LOW prior to STR1 (note 3)	t_{CSL}	52	60	–	CLOX periods

NOTES TO THE CHARACTERISTICS

1. $V_I = -0{,}3$ to $+6{,}5$ V; $T_{amb} = 25\ ^{\circ}C$.

2. All outputs, except XTAL2, are short-circuit protected to V_{DD1} and V_{SS}. Output XTAL2 is protected to V_{SS} only.

3. Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{CLEC}$ period is twice the CLOX period.

4. Output load capacitance is 50 pF.

5. XTAL1 (pin 8) is driven by an external clock.

6. Output load capacitance is 30 pF on STR1, STR2 outputs.
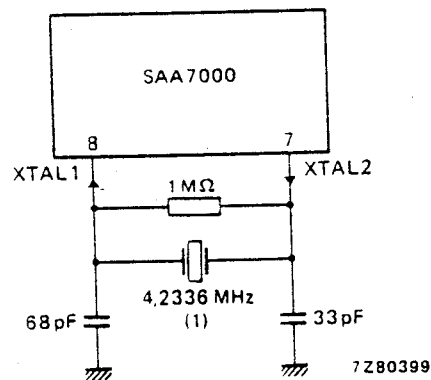
(1) Catalogue number of crystal is 6416 009 00111.

Fig. 3 Crystal oscillator circuit.

Fig. 4 Typical input waveforms.
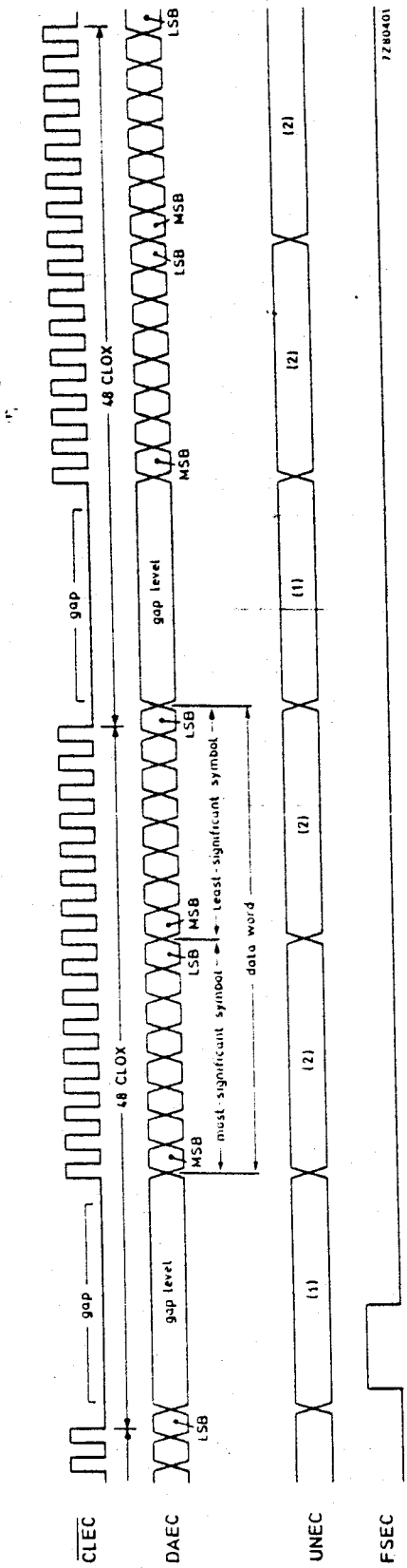
(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.
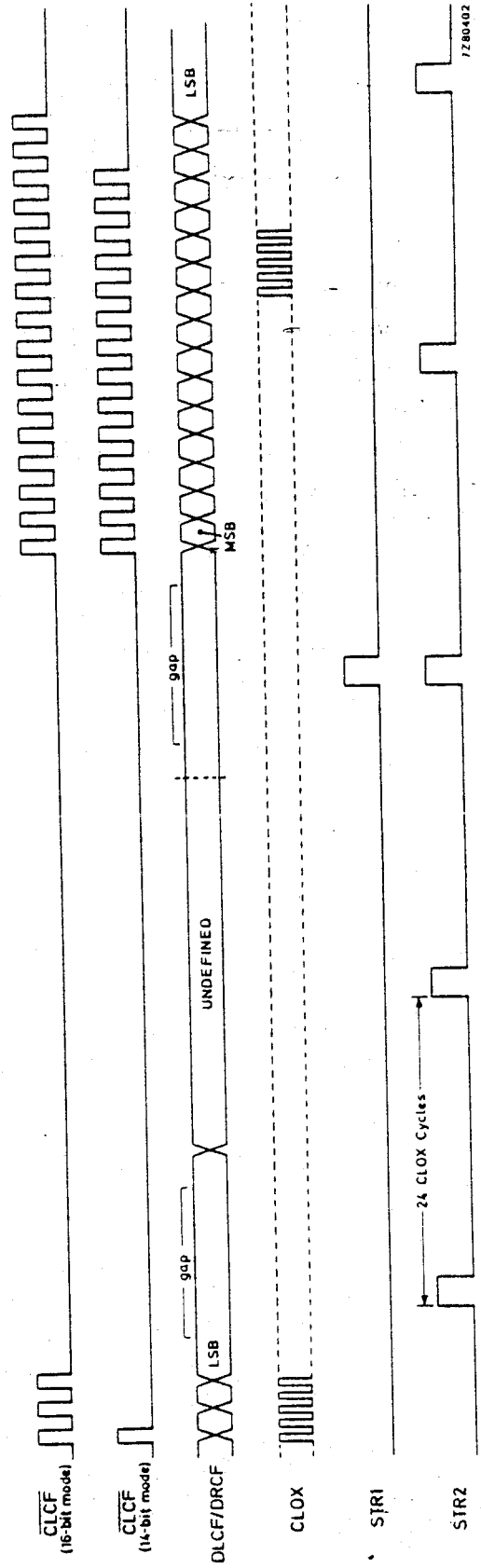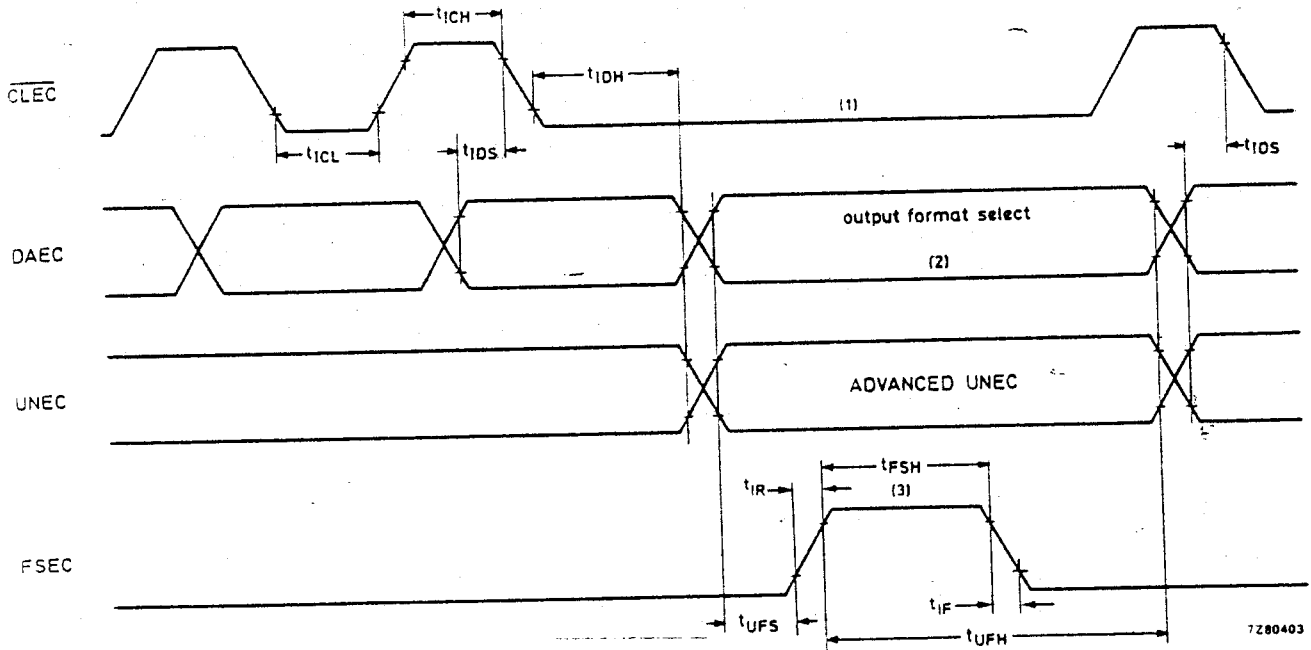

Fig. 5 Typical output waveforms.

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COMPACT DISC CIRCUIT

3

(1) $\overline{CLEC}$ remains LOW for a minimum period of approximately 16 CLOX periods.

(2) Data during this time is used to determine the format of the output from SAA7000; when DAEC is HIGH a two's complement format is selected, when LOW an offset binary format is selected.

(3) Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{CLEC}$ period is twice the CLOX period.

Fig. 6 Input waveforms. Reference levels are 0,8 V and 2,4 V; t_{IR} and t_{IF} apply to FSEC waveform only.
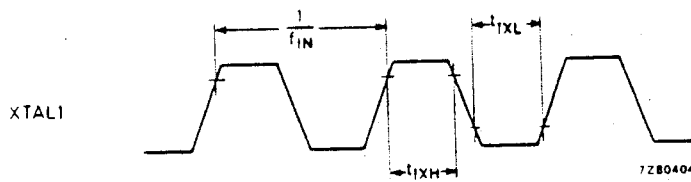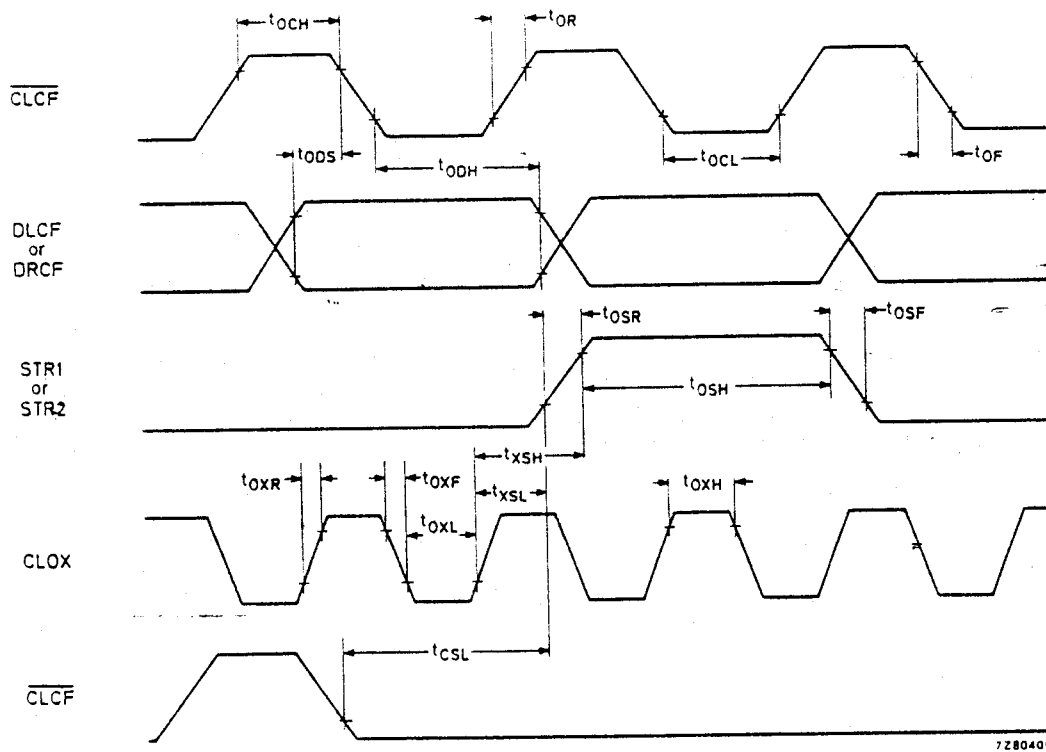

Fig. 7 Optional clock input waveform at XTAL1 (pin 8).

Fig. 8 Output waveforms. Reference levels are 0,8 V and 2,4 V. Output loadings on STR1 and STR2 are 30 pF; output loadings on CLOX, $\overline{\text{CLCF}}$, DLCF and DRCF are 50 pF.