Main application areas of digital audio converters

Type	Description	Home hi-fi	Portable hi-fi	Car	Multimedia
SAA7360GP	high-performance bitstream ADC	✓		✓	
SAA7366T	economy bitstream ADC	✓		✓	
SAA7367T	economy bitstream ADC	✓		✓	
TDA1305T(AT)	bitstream/CC filter-DAC	✓	✓	✓	✓
TDA1306T	CC filter-DAC	✓	✓	✓	✓
TDA1307	high-performance bitstream digital filter	✓			
TDA1309H	low-voltage bitstream/CC ADC + DAC	✓	✓	✓	
TDA1310A(AT)	continuous calibration DAC with current output	✓	✓	✓	✓
TDA1311A(AT)	continuous calibration DAC with voltage output	✓	✓	✓	✓
TDA1312A(AT)	continuous calibration DAC with voltage output	✓	✓	✓	
TDA1313(T)	continuous calibration DAC with voltage output	✓	✓	✓	
TDA1314T	quad sign-magnitude filter-DAC with voltage output	✓	✓	✓	
TDA1386T	CC filter-DAC	✓	✓	✓	
TDA1387T	continuous calibration DAC with current output	✓	✓	✓	✓
TDA1388T	bitstream/CC filter DAC	✓			✓
TDA1541A	high-performance 16-bit DAC	✓			
TDA1541A/R1	high-performance 16-bit DAC	✓			
TDA1541A/S1	single crown 16-bit DAC	✓			
TDA1541A/S2	double crown 16-bit DAC	✓			
TDA1543(T)	economy 16-bit DAC	✓		✓	
TDA1545A(AT)	continuous calibration DAC with current output	✓	✓	✓	
TDA1547	top-grade BiMOS bitstream DAC	✓			
TDA1548T	low-voltage bitstream/CC filter-DAC with DSP features		✓	✓	
TDA1549(T)	bitstream/CC DAC	✓	✓	✓	
UDA1309H	low-power stereo bitstream DAC	✓			
UDA1320TZ	low-voltage bitsream filter DAC		✓	✓	
UDA1321	USB DAC				✓
UDA1322TS	low-voltage bitstream DAC with DSP features		✓		
UDA1324TS	ultra low-voltage bitstream filter DAC		✓		
UDA1325	USB ADC/DAC				✓
UDA1340M	low-voltage stereo filter ADC/DAC with DSP	✓	✓		
UDA1341TS	low-voltage stereo filter ADC/DAC with DSP	✓	✓		

Survey of stereo audio DACs (ranked by typical THD + N at 0 dB performance per category)

Type	Description	Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB dB(%) [4]	Typ. SNR (dB) [4]	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
Bitstream DAC										
TDA1547[1]	top-grade BiMOS bitstream DAC	24	1-bit, 192f_s	-101(0.0009)	-51(0.02)	113	1.0	5 ±10%	800	DIL32S
Bitstream/continuous calibration DACs										
TDA1549T [5]	bitstream/CC DAC	24	"S", 4f_s, 18-bit	-90(0.003)	-50(0.32)	110	1.5	3.4 to 5.5	35	SO16
16-bit DACs										
TDA1541A/S2[3]	double crown 16-bit DAC	1	I^2S, up to 8f_s	-97(0.0014)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/S1[3]	single crown 16-bit DAC	1	I^2S, up to 8f_s	-95(0.0018)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A[3]	high-performance 16-bit DAC	1	I^2S, up to 8f_s	-95(0.0018)	-42(0.79)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/R1[3]	high-performance 16-bit DAC	1	I^2S, up to 8f_s	-95(0.0018)	-43(0.7)	112	(4.0)	5 ±10%	700	DIL28
TDA1543(T)	economy 16-bit DAC	1	I^2S, up to 4f_s	-75(0.018)	-33(2.2)	96	(2.3)	3 to 8	250	DIL8, SO16
Continuous calibration DACs										
TDA1313(T)[5]	continuous calibration DAC with voltage output	1	"S", up to 8f_s	-88(0.004)	-38(1.3)	98	4.2	3 to 5.5	30	DIL16, SO16
TDA1545A(AT)	continuous calibration DAC with current output	1	"S", up to 4f_s	-88(0.004)	-35(1.7)	101	(1.0)	3 to 5.5	6	DIL8, SO8
TDA1387T	continuous calibration DAC with current output	1	I^2S, up to 4f_s	-88(0.004)	-35(1.7)	98	(1.0)	3 to 5.5	28	DIL8, SO8
TDA1312A(AT)[5]	continuous calibration DAC with voltage output	1	"S", up to 8f_s	-68(0.04)	-33(2)	92	2.0	4 to 5.5	8	DIL8, SO8
TDA1311A(AT)[5]	continuous calibration DAC with voltage output	1	"S", up to 4f_s	-68(0.04)	-33(2.2)	92	2.0	4 to 5.5	8	DIL8, SO8
TDA1310A(AT)	continuous calibration DAC with current output	1	"S", up to 4f_s	-65(0.05)	-33(2.2)	95	(1.0)	3 to 5.5	6	DIL8, SO8

NOTES:

1. measured with SAA7350 and 20-bit input; 2. includes digital filter; 3. high sound quality: dynamic element matching (DEM);
4. A-weighting; 5. includes I/V converter.

TDA1541A/R1/S1/S2

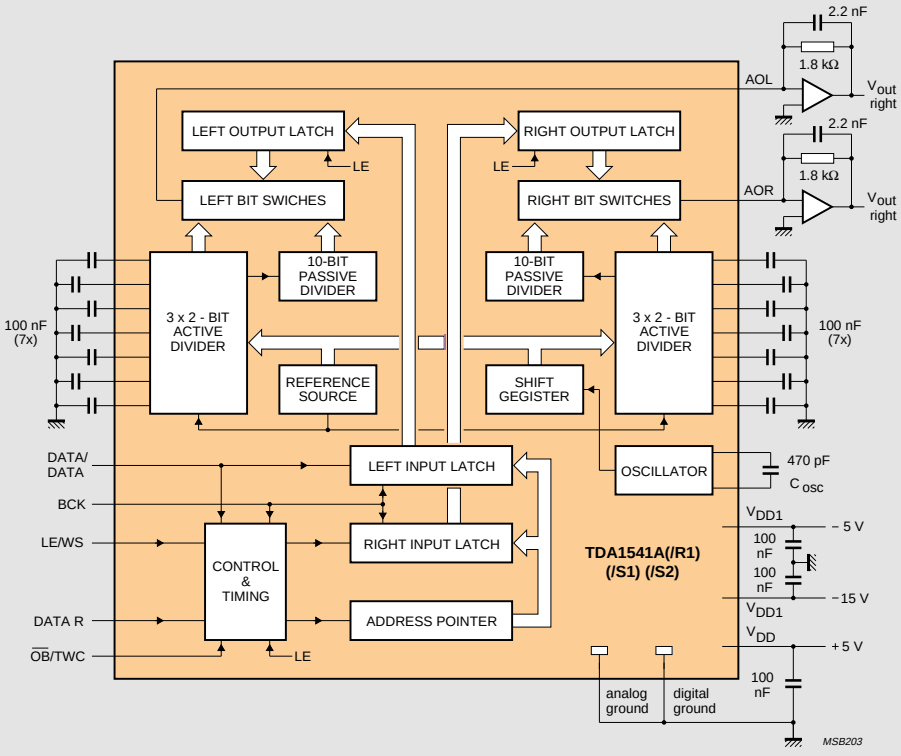
High-performance 16-bit DAC

- **Dynamic Element Matching (DEM)**
- **$4f_s$ or $8f_s$ oversampling**
- **I^2S input data format, up to $8f_s$**
- **TTL compatible inputs**
- **Marked with single crown (TDA1541A/S1 only)**
- **Marked with double crown (TDA1541A/S2 only)**

These monolithic integrated dual 16-bit digital-to-analogue converters are specifically designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

With this range of DACs, the ten lowest bits are derived from a reference current while the six highest bits are generated by time-averaging in the Dynamic Element Matching (DEM) parts. For a full description the DEM technique.

	TDA1541A/S2	TDA1541A/S1	TDA1541A	TDA1541A/R1
Typ. THD + N at full-scale at 0 dB	–97 dB	–95 dB	–95 dB	–95 dB
Typ. THD + N at –60 dB	–47 dB	–47 dB	–42 dB	–43 dB
Channel separation	98 dB	98 dB	98 dB	98 dB
Typ. signal-to-noise ratio	112 dB	112 dB	112 dB	112 dB
Full-scale output current	4.0 mA	4.0 mA	4.0 mA	4.0 mA
Package	DIL28	DIL28	DIL28	DIL28



SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB; note 3, Fig. 3, 4	– –	–95 0.0018	–90 0.0032	dB %
THD	total harmonic distortion	including noise at –60 dB; note 3, Fig. 3, 4	– –	–42 0.79	– –	dB %
t_{cs}	settling time ±1 LSB		–	0.5	–	µs
α	channel separation		90	98	–	dB
$\lvert d_{IO}\rvert$	unbalance between outputs	note 4	–	< 0.1	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	–	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	–	–76	–	dB
SSVR	supply voltage ripple rejection	V_{DD1} = –5 V; note 4	–	–84	–	dB
SSVR	supply voltage ripple rejection	V_{DD2} = –15 V; note 4	–	–58	–	dB
S/N	signal-to-noise ratio	at bipolar zero	–	110	–	dB
S/N	signal-to-noise ratio	at full scale	98	104	–	dB
Timing (Fig. 5 and 6)						
t_r	rise time		–	–	32	ns
t_f	fall time		–	–	32	ns
t_{CY}	bit clock cycle time		156	–	–	ns
t_{HB}	bit clock HIGH time		46	–	–	ns
t_{LB}	bit clock LOW time		46	–	–	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	–	–	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	–	–	ns
$t_{SU;DAT}$	data set-up time		32	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		0	–	–	ns
$t_{HD;WS}$	word select hold time		0	–	–	ns
$t_{SU;WS}$	word select set-up time		32	–	–	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.
2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

TDA1541A	bit 1-16	E_{dL} < 1 LSB
TDA1541A/R1	bit 1-16	E_{dL} < 2 LSB
TDA1541A/S1	bit 1-7	E_{dL} < 0.5 LSB
	bit 8-15	E_{dL} < 1 LSB
	bit 16	E_{dL} < 0.75 LSB