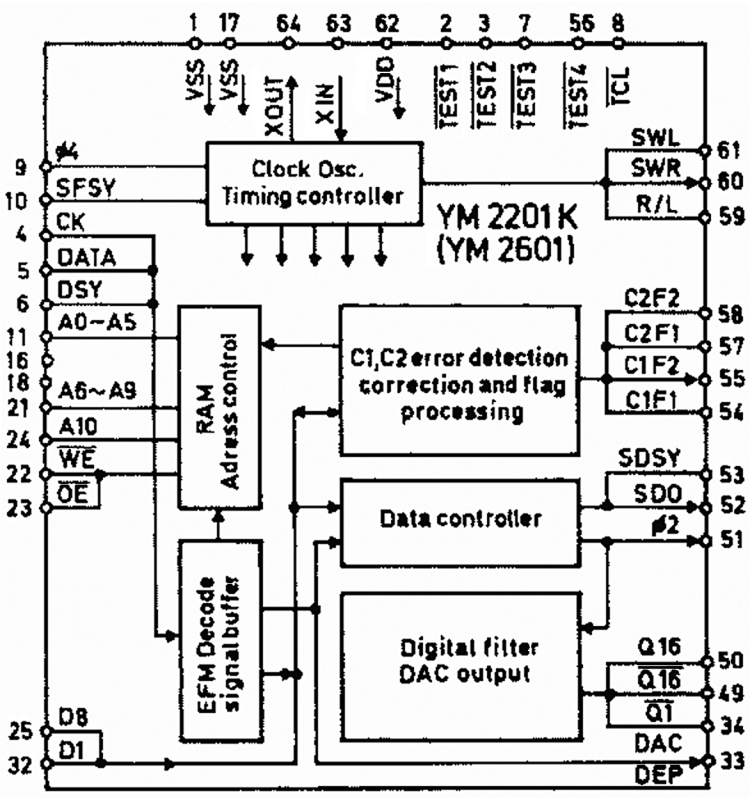
1
17
64
63
62
2
3
7
56
8
VSS
VSS
XOUT
XIN
VDD
TEST1
TEST2
TEST3
TEST4
TCL
Clock Osc.
Timing controller
YM 2201K
(YM 2601)
SWL
SWR
R/L
61
60
59
9
10
4
5
6
11
16
18
21
24
22
23
SFSY
CK
DATA
DSY
A0~A5
A6~A9
A10
WE
OE
RAM
Adress control
C1,C2 error detection
correction and flag
processing
C2F2
C2F1
C1F2
C1F1
58
57
55
54
SDSY
SDO
Data controller
53
52
51
EFM Decode
signal buffer
Digital filter
DAC output
Q16
Q16
Q1
DAC
DEP
50
49
34
33
25
32
D8
D1

Terminal Functions

Terminal number	Terminal code	I/O	Outline of functions
1 17	VSS VSS	I I	These are the grounding terminals.
2 3 7 8	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$ $\overline{\text{TEST 3}}$ $\overline{\text{TCL}}$	I + I + I + I +	These test terminals are ungrounded, and contain pull-up resistors.
4	CK	I	This is the VCO clock (average 4.3218MHz) input terminal, connected to the SVC output.
5	DATA	I	This is the serial signal input terminal for the 8 bit EFM demodulation signals and the 5 bit control signals, connected to the SVC output.
6	DSY	I	This is the synchronization signal input terminal for the serial signals (see above), connected to the SVC output.
9	ϕ4	0	This is the crystal clock (4.3218MHz) output terminal, connected to the SVC input.
10	$\overline{\text{XFSY}}$	I/0	This is the frame synchronization signals (7.35kHz) output terminal, connected to the SVC input. (During test operations, the synchronization can be resynchronized by setting this terminal to the "L level".)
11 12 13 14 15 16 18 19 20 21 24	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	0 0 0 0 0 0 0 0 0 0 0	These are the address output terminals, connected to the RAM address terminals.
22	$\overline{\text{WE}}$	0	This is connected to the RAM WE terminal. When a "L level" signal is registered, the RAM will be set to the WRITE mode.
23	$\overline{\text{OE}}$	0	This is connected to the RAM OE terminal. When a "L level" signal is registered, the RAM will be set to the READ mode.
25 26 27 28 29 30 31 32	D8 D7 D6 D5 D4 D3 D2 D1	I/0 I/0 I/0 I/0 I/0 I/0 I/0 I/0	These are connected to the RAM data terminals. The output mode is set when the cycle at the data input terminal is WE = "L", and the input mode is set when the cycle is WE = "H".
33	DEP	0	This is the output terminal for the audio frequency characteristics switching signals of the audio filter. The emphasis will be required when "H" is registered.

Terminal number	Terminal code	I/O	Outline of functions
34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	$\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$ $\overline{Q4}$ $\overline{Q5}$ $\overline{Q6}$ $\overline{Q7}$ $\overline{Q8}$ $\overline{Q9}$ $\overline{Q10}$ $\overline{Q11}$ $\overline{Q12}$ $\overline{Q13}$ $\overline{Q14}$ $\overline{Q15}$ $\overline{Q16}$ Q16	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Connected to the DAC input, the parallel signals are output by way of the internal digital filter form these terminals. The output is in alternation from the left and right channels. The output rate for each channel is 88.2kHz. Connect either Q16 or ($\overline{Q16}$), according to the DAC to be used.
51	$\phi 2$	0	This is the crystal clock (2.1609MHz) output.
52	SDO	I/0	This is the serial signal output for the DAC. Using a $\phi 2$ clock beat rate, the signals are output from LSB in the order of L channel 24 bit — R channel 25 bit.
53	SDSY	0	This is the synchronization signal output for the above serial signals. The level is "H" for L channel and "L" for R channel.
56	TEST	I+	This test terminal contains pull-up resistors, and is normally disconnected. Using a "L" signal, it is also possible to input serial signals with the same format as the above serial signals from the SDO terminal into the digital filter.
54 55 57 58	C1F1 C1F2 C2F1 C2F2	0 0 0 0	This monitor output terminal depicts the C1 and C2 error correction operation mode.
59	R/L	0	This is the output terminal for the channel allocation signal of the DAC analog output. "H" is for the R channel, and "L" is for the L channel.
60 61	SWR SWL	0 0	This is the degliche signal for the respective channels of the DAC analog output.
62	VDD	I	This is the +5V power supply terminal.
63 64	XIN XOUT	I 0	A crystal oscillator is connected between these terminals, which are used for the crystal clock (8.6436MHz) oscillation.