YM3404B

(CDDF)

2-Channel 4-times Oversampling Digital Filter

■ OUTLINE

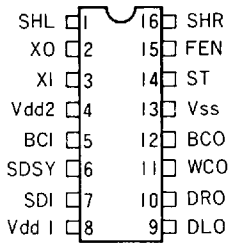
The YM3404B (CDDF) is a super-high performance 4-times oversampling digital filter for use with the digital audio systems developed by Yamaha.

It is connectable directly to LSI, SPCII, SPCIII, DIT, DIR, etc. for digital audio systems, and can exhibit its exellent performance through simple procedures.

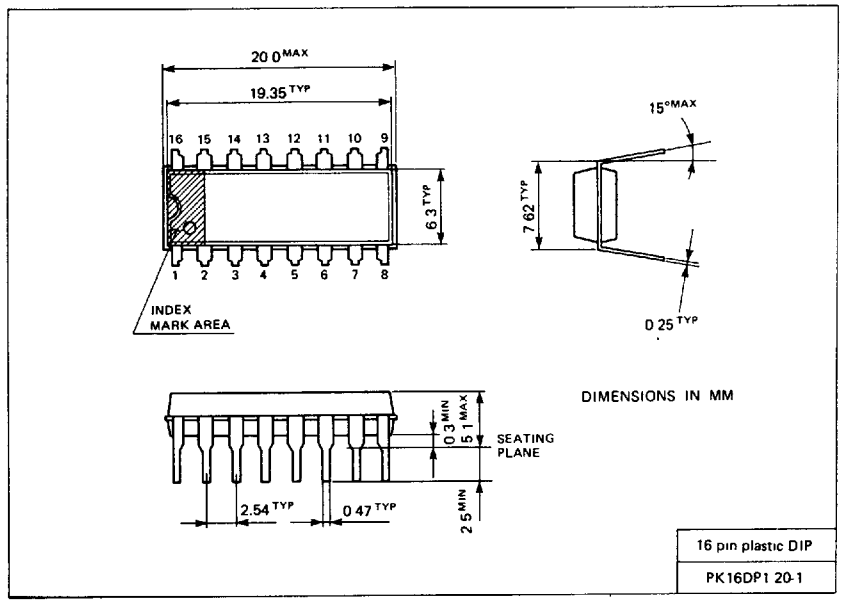
■ FEATURES

- 4-times oversampling in two channels
- Linear phase FIR type filters connected in two vertical stages
  - 1'st filter: 225-order FIR filter
  - 2'nd filter: 41-order FIR filter
- 19 × 18 bits multiplier built in
- Floating point multiplier and accumlater having a coefficient of 18 bits
- Overflow limiter built in
- Filter characteristics (fs=44.1 kHz)
  - Pass band ripple: Within ±0.0001 dB at 0 to 20 kHz
    (Within quatization error in 16 bits)
  - Stop band attenuation: At least 100 dB at 24.1 to 64.1 kHz
    At least 99 dB at 64.1 kHz and higher
- High precision oscillator specially designed for use with the filter
- Clock providing 8.6426 MHz output for SPCII and SPCIII
- C-MOS type processor
- Single 5 V power supply
- 16-pin type DIP package

■ TERMINAL DIAGRAM



■ TERMINAL FUNCTIONS

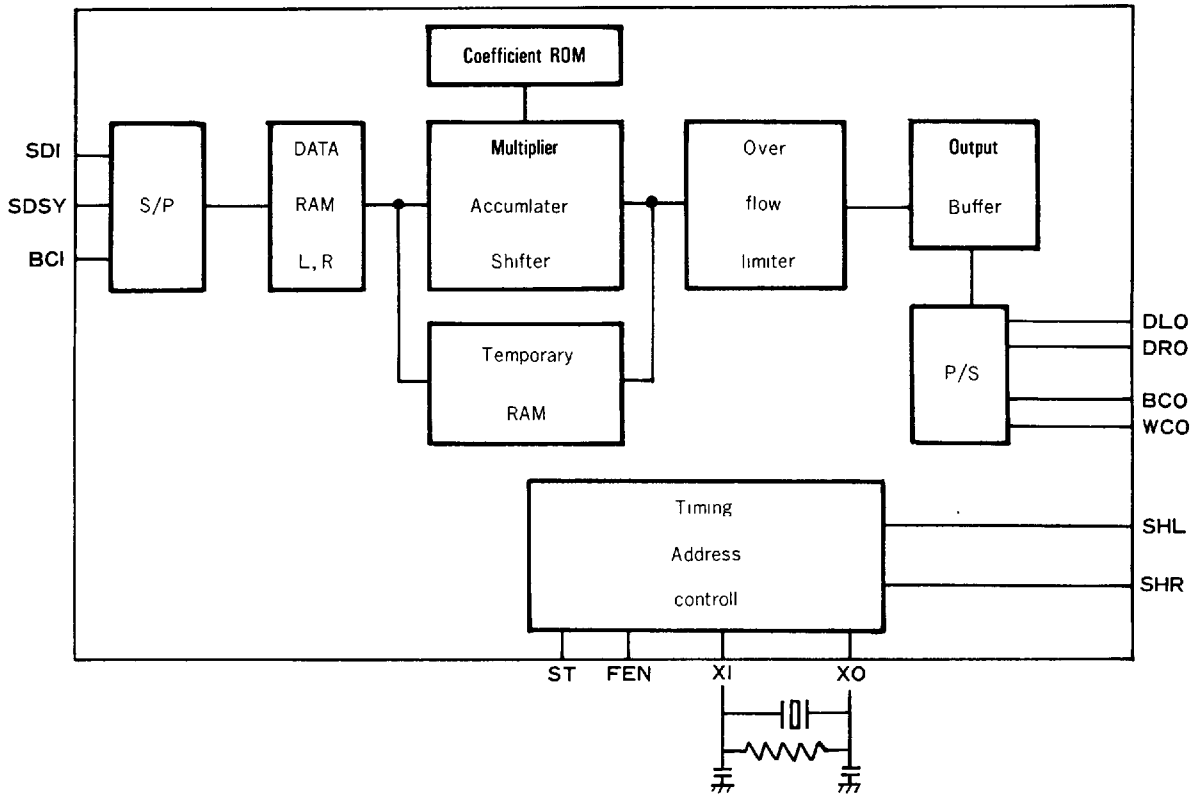


■ EXTERNAL DIMENSIONS

Terminal Name	Pin No.	I/O	Outline of Functions
SHL	1	O	At 1 DAC (ST='L'): Degricher signal for Lch At 2 DAC (ST='H'): Degricher signal for L/Rch
XO	2	O	Crystal oscillation between XI-XO. At 392 fs (FEN='L'): 17.2872 MHz
XI	3	I	At 384 fs (FEN='H'): 16.9344 MHz (XI can receive direct external input.)
Vdd2	4		+5 V power supply terminal for crystal oscillation and degricher signal
BCI	5	I	Bit clock input terminal for input data
SDSY	6	I	Clock signal indicating L/Rch discrimination of input data and input timing
SDI	7	I	Data input terminal
Vddl	8		+5 V power supply terminal for the digital signal system
DLO	9	O	At 1 DAC (ST='L'): L and Rch data output terminal At 2 DAC (ST='H'): Lch data output terminal
DRO	10	O	Rch data output terminal
WCO	11	O	Word clock for output data DLO and DRO
BCO	12	O	Bit clock for the output data. System clock output terminal for SPCII and SPCIII.
Vss	13		GND terminal
ST	14	I	1 DAC/2 DAC switching terminal (1 DAC='L', 2 DAC='H')
FEN	15	I	System clock switching terminal (392fs='L', 384FS='H')
SHR	16	O	Rch degricher signal at 1 DAC

* Vdd 1 and Vdd 2 are internally connected.

■ BLOCK DIAGRAM



■ OUTLINE OF FUNCTIONS

The functions of the 2-channel 4-times oversampling digital filter are obtained by connecting linear phase type of FIR filters at two vertical stages: 225-order FIR filter at the first stage and 41-order FIR filter at the second stage.
The built-in multiplier is of 19 × 18 bits type and comprises an overflow limiter. It performs multiplication and addition with floating point in 18 bits of coefficient wordlength.
Theoretical filter characteristics are: (fs=44.1 kHz)

Ripple at pass band (0 to 20 kHz): Within 0.0001 dB or below quantization error in 16 bits
Attenuation at stop band (24.1 kHz): At least 99 dB

The sampling digital filter can process input of MSB first signal in 16 bits 2 channels: 96fs or 98fs depending on FEN terminal setting.
(BCI, SDSY and SDI are synchronized completely with the XI clock, and should be transmitted with clock signals obtained by dividing frequency of XI. No restrictions are posed on phase relationship with XI.)
Output is obtainable in the signal format of 1 DAC or 2 DAC depending on setting of ST. Extended portion of the internal multiplication data is output to the two bits (−2) and (−1) below LSB. The data is unnecessary for operation of the sampling digital filter in 16 bits. The filter is so designed as to minimize rounding error at any omitting position.

Filter characteristics (theoretical values)

	fs=at 44.1KHz	fs standard
Ripple at pass band	within 0.0001dB	
Pass band	0~20KHz	$0\sim\frac{20}{44.1}\cdot fs$
Attenuation at stop band	over −100dB	
Stop band	24.1~156.4KHz	$\frac{24.1}{44.1}\cdot fs\sim\frac{156.4}{44.1}\cdot fs$

	fs=at 44.1KHz	fs standard
Slope characteristics	20KHz	$\frac{20}{44.1}\cdot fs$
	−0.00013dB	
	24.1KHz	$\frac{24.1}{44.1}\cdot fs$
	−102dB	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	Vdd	−0.3	+7.0	V
Input voltage	VI	−0.3	Vdd+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

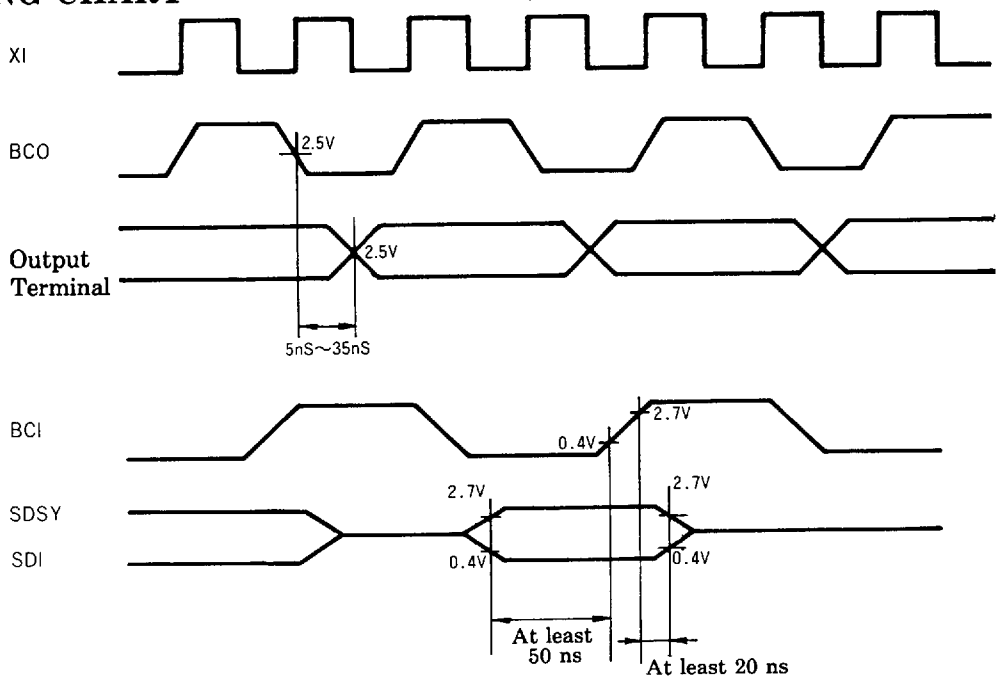
■ RECOMMENDED WORKING CONDITIONS

Item	Symbol	Minimum	Standard	Maximum	Unit
Power supply voltage	VDD	4.75	5.0	5.25	V
Clock frequency	XIN	12.2	16.93	18.5	MHz
Working temperature	Top	0	25	70	°C

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 ± 0.25 V)

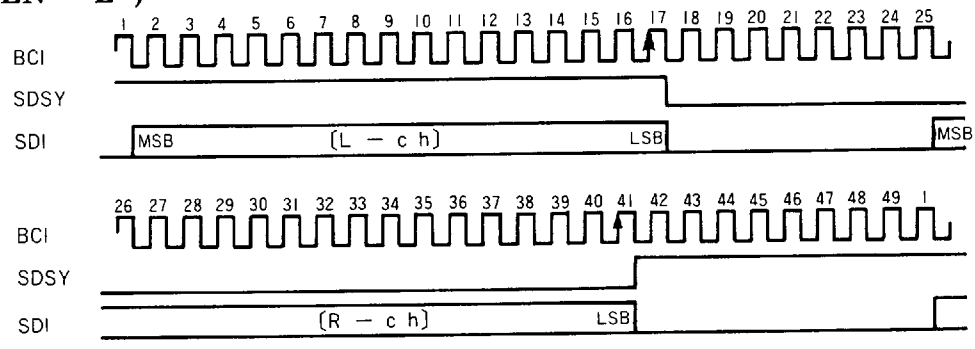
Item	Symbol	Condition	Minimum	Standard	Maximum	Unit
Power consumption	W	Vdd=+5V		200	270	mW
Input voltage H level (XI, FEN, ST) (BCI, SDSY, SDI)	VIH		 3.5 2.7		 Vdd Vdd	 V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		Vdd	V
Output voltage L level	VOL		0		0.4	V
Output delay (delay from BCO)			5		35	nsec
Input data setup time (Rise of BCI)			50			nsec
Input data hold time (Rise of BCI)			20			nsec
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ TIMING CHART

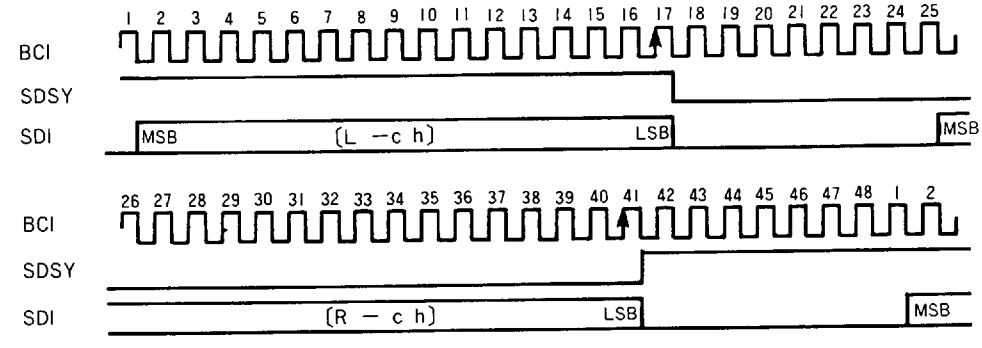


■ INPUT SIGNAL FORMAT

■ 98fs (FEN = "L")



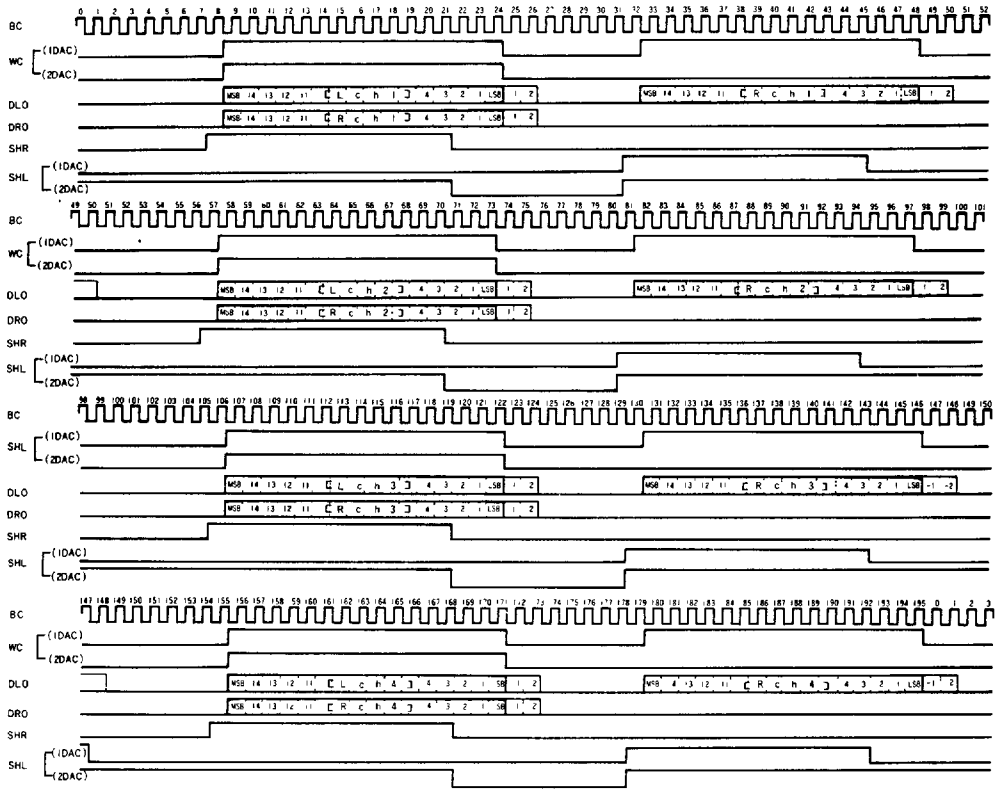
■ 96fs (FEN = "H")



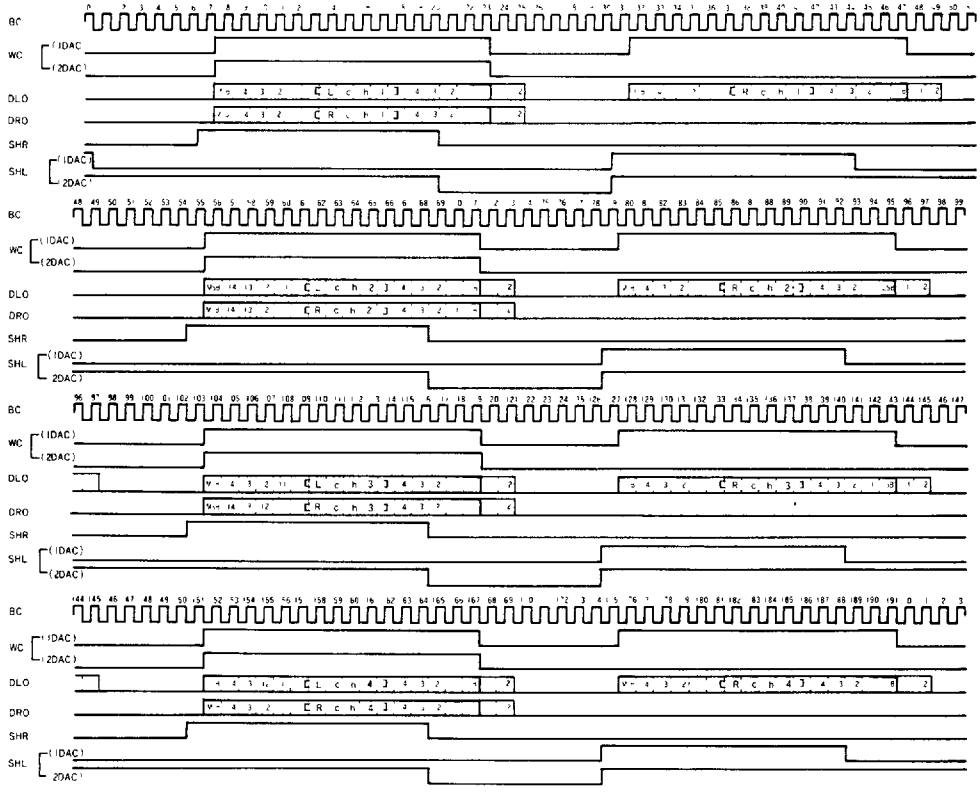
NOTE: Calculation start in the LSI is triggered by rise of SDSY.
Therefore, the interval between L and R may be set at width of any number of the clock pulses. Both SDSY and SDI are synchronized at their rises.

■ OUTPUT SIGNAL FORMAT

98fs (FEN = "L")

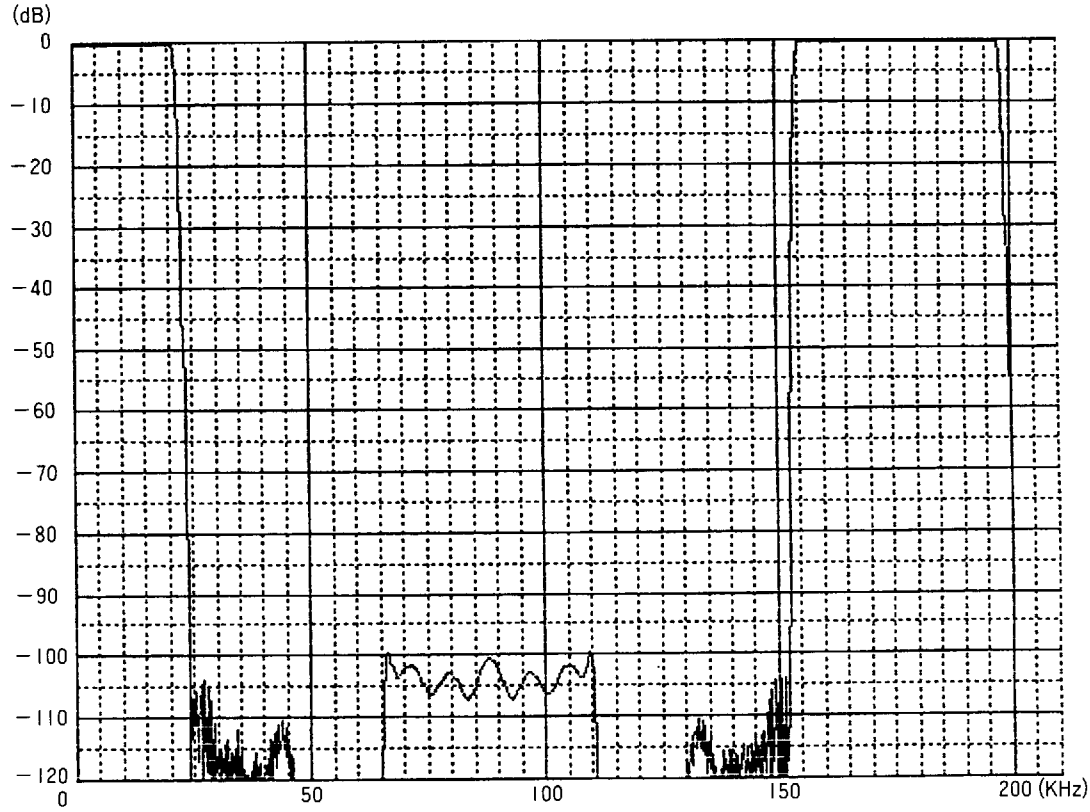


96fs (FEN = "H")

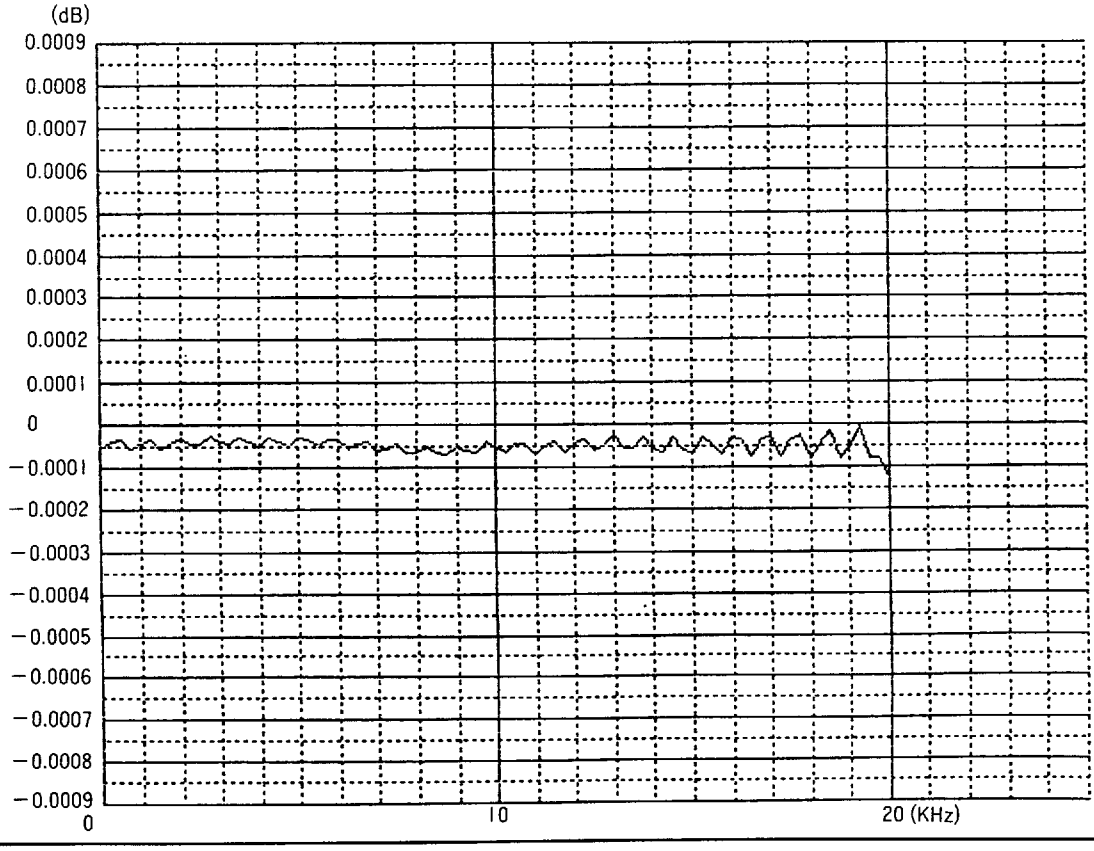


■ CHARACTERISTICS FOR REFERENCE

OVERALL CHARACTERISTIC (theoretical value)

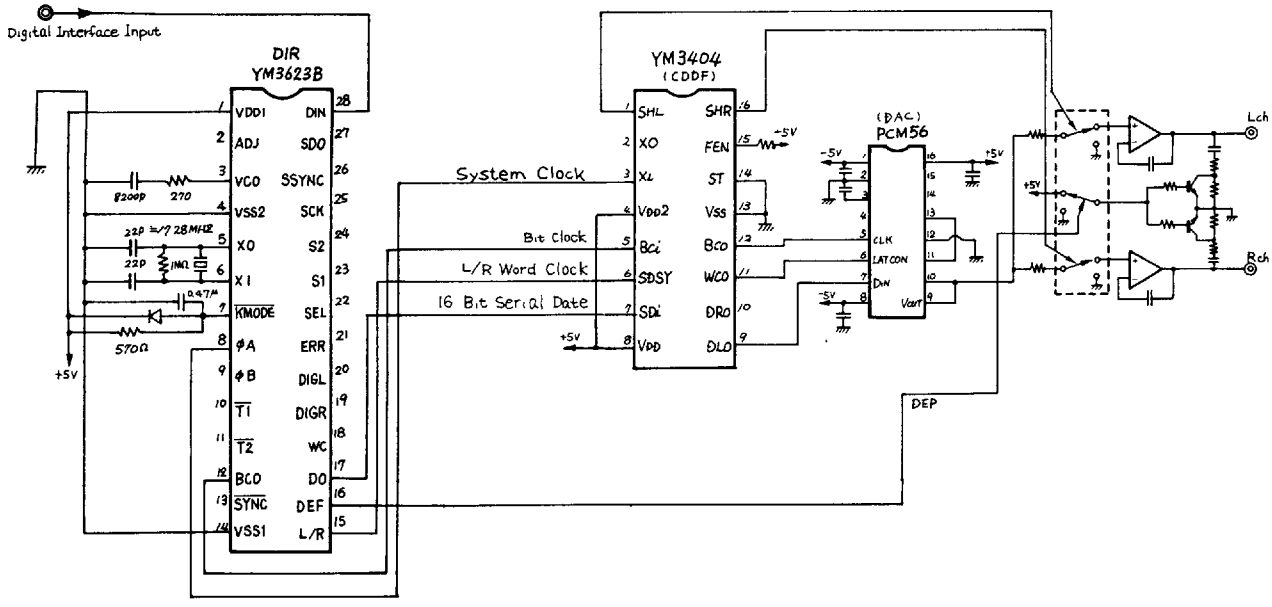


OVERALL PASS BAND CHARACTERISTIC (theoretical value)

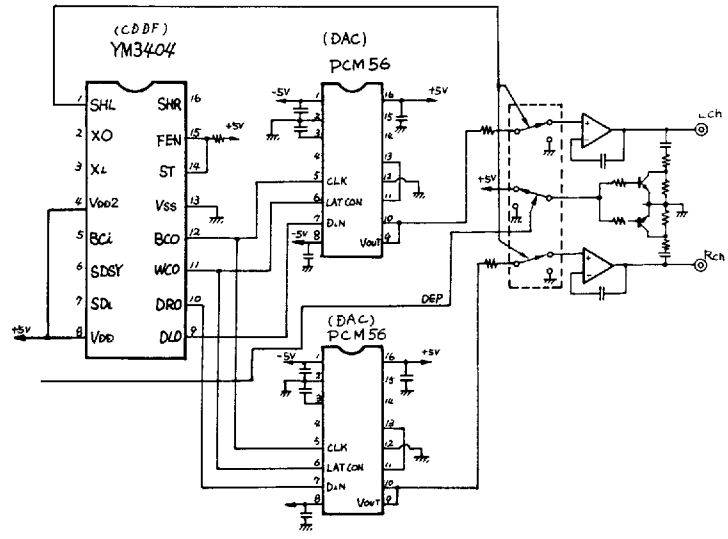


■ EXAMPLES OF APPLICATION

1 DAC System



2 DAC System



The specifications of this product are subject to improvement changes without prior notice.

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